



User Manual

AIMB-589

**Micro-ATX Motherboard
Intel® Core™ Ultra Series 2
Processors (codename: Arrow
Lake-S)**

ADVANTECH

Enabling an Intelligent Planet

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Part No. 2006058900

Printed in China

Edition 1

May 2026

A Message to the Customer

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

CPU Compatibility

Processor Number	Code Name	Max_TDP	Cores/ Threads	Max Speed (GHz)	Smart Cache (L3)	Lithography	ADVANTECH P/N	Result
Intel Core Ultra 9 285	Arrow Lake-S	65W	8P+16E/24T	5.6/4.6	36MB	TSMC N3B	96MPU-285-24E	PASS
Intel Core Ultra 9 285T	Arrow Lake-S	35W	8P+16E/24T	5.6/4.6	36MB	TSMC N3B	96MPU-285T-24E	PASS
Intel Core Ultra 7 265	Arrow Lake-S	65W	8P+12E/20T	5.3/4.6	30MB	TSMC N3B	96MPU-265-20E	PASS
Intel Core Ultra 7 265T	Arrow Lake-S	35W	8P+12E/20T	5.3/4.6	30MB	TSMC N3B	96MPU-265T-20E	PASS
Intel Core Ultra 5 245	Arrow Lake-S	65W	6P+8E/14T	5.1/4.5	24MB	TSMC N3B	96MPU-245-14E	PASS
Intel Core Ultra 5 245T	Arrow Lake-S	35W	6P+8E/14T	5.1/4.5	24MB	TSMC N3B	96MPU-245T-14E	PASS
Intel Core Ultra 5 225	Arrow Lake-S	65W	6P+4E/10T	4.9/4.4	20MB	TSMC N3B	96MPU-225-10E	PASS
Intel Core Ultra 5 225T	Arrow Lake-S	35W	6P+4E/10T	4.9/4.4	20MB	TSMC N3B	96MPU-225T-10E	PASS

ECC Memory Compatibility

Category	Speed	Capacity	Vendor	Module P/N	Chip P/N	ADVANTECH P/N	ECC	Result
DDR5	5600	16GB	Advantech	SQR-UD5N16G5K6SEP8	SEC 346 K4RAH08 6VP BCWM	SQR-UD5N16G5K6SEP8	ECC	PASS
DDR5	5600	32GB	Advantech	SQR-UD5N32G5K6SEP8	SEC 346 K4RAH08 6VP BCWM	SQR-UD5N32G5K6SEP8	ECC	PASS
DDR5	6400	32GB	Advantech	AQD-D5V32GE64-HB	H5CG48AH BD X018 446V	AQD-D5V32GE64-HB	ECC	PASS
DDR5	5600	16GB	Advantech	AQD-D5V16GE56-SB	SEC 337 K4RAH08 6VP BCWM	AQD-D5V16GE56-SB	ECC	PASS
DDR5	4800	16GB	Advantech	AQD-D5V16GE48-SB	SEC 246 K4RAH08 6VB BCQK	AQD-D5V16GE48-SB	ECC	PASS
DDR5	4800	32GB	Advantech	AQD-D5V32GE48-SB	SEC 246 K4RAH08 6VB BCQK	AQD-D5V32GE48-SB	ECC	PASS

Non-ECC Memory Compatibility

Category	Speed	Capacity	Vendor	Module P/N	Chip P/N	ADVANTECH P/N	ECC	Result
DDR5	5600	8GB	Advantech	SQR-UD5N8G5K6HNGAG	H5CG46A GBD X017 351V	SQR-UD5N8G5K6HNGAG	N	PASS
DDR5	5600	16GB	Advantech	SQR-UD5N16G5K6HNAG	H5CG48A GBD X018 421V	SQR-UD5N16G5K6HNA G	N	PASS
DDR5	5600	32GB	Advantech	SQR-UD5N32G5K6HNAG	H5CG48A GBD X018 421V	SQR-UD5N32G5K6HNA G	N	PASS
DDR5	6400	48GB	Advantech	SQR-UD5M48G6K4HNG	H5CG08M HBD X021 301A	SQR-UD5M48G6K4HNG	N	PASS
DDR5	6400	16GB	Advantech	AQD-D5V16GN64-HB	H5CG48AH BD X018 441A	AQD-D5V16GN64-HB	N	PASS
DDR5	5600	16GB	Advantech	AQD-D5V16GN56-SB	SEC 343 K4RAH08 6VP BCWM	AQD-D5V16GN56-SB	N	PASS
DDR5	5600	32GB	Advantech	AQD-D5V32GN56-SB	SEC 346 K4RAH08 6VP BCWM	AQD-D5V32GN56-SB	N	PASS
DDR5	6400	32GB	Advantech	AQD-D5V32GN64-HB	H5CG48AH BD X018 448V	AQD-D5V32GN64-HB	N	PASS
DDR5	4800	16GB	Advantech	AQD-D5V16GN48-SB	SEC 213 K4RAH08 6VB BCQK	AQD-D5V16GN48-SB	N	PASS

Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- 1 x AIMB-589 Motherboard
- 1 x SATA HDD cable
- 1 x I/O port bracket
- 1 x startup manual
- 1 x warranty card
- 2 x Screw (M2.5*4L)

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the AIMB-589 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-589, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

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Chapter 1

General Introduction

1.1 Introduction

The AIMB-589 is powered by Intel® Core™ Ultra Series 2 Processors (LGA1851, up to 65W TDP), delivering robust performance and power efficiency for a wide range of industrial applications. This Micro-ATX motherboard adopts the Intel® W880 or Q870 chipset and supports up to 48GB of dual-channel DDR5 5600 MT/s memory across four 288-pin UDIMMs/CUDIMMs slots. It features extensive I/O connectivity, including 6 COM ports, 1 x USB4 Type-C, support DisplayPort1.4 Alt. Mode and PD 100W output, 6 x USB3.2 Gen2 x1 and 2 x USB3.2 Gen1 x1, two Ethernet ports supporting 1 GbE and two Ethernet ports supporting 2.5 GbE. For storage and expansion, the AIMB-589 offers 8 SATA III ports and 3 M.2 slots, including two M-Key slots for NVMe SSDs and an E-Key slot for wireless connectivity such as Wi-Fi or Bluetooth. The motherboard supports high-performance graphics with Intel Enhanced Intel® Xe LPG architecture, providing up to one HDMI 2.1 TMDS up to 4096 x 2160 @60Hz, two DP 1.4 up to 4096 x 2160 @120Hz and one eDP1.4, up to 4096 x 2160 @60Hz (Internal pin header).

1.2 Features

- Intel® Core™ Ultra Series 2 Processors, max. 24 Core. Support W880/Q870 chipsets
- Up to 192GB DDR5 UDIMMs/CUDIMMs for data transfer
- 2 x 2.5GbE LAN and 2 x GbE LAN for digital devices
- 1 x USB4 Type-C, support DisplayPort1.4 Alt. Mode and PD 100W output, 8 x USB3.2, 4 x USB2.0
- 2 x M.2 M-Key 2280 for NVMe SSD Accommodate 2 double-deck GPU cards by PCIe x16 slots (x8 lanes)

1.3 Specifications

1.3.1 System

- **CPU:** Supports Intel® Core™ Ultra Series 2 Processors (LGA1851, up to 65W TDP)
- **BIOS:** AMI EFI 512 Mbit SPI BIOS.
- **System chipset:** Intel® W880/Q870
- **SATA hard disk drive interface:**
 - Eight on-board SATA connector with a data transmission rate up to 6 GB/s
 - 2 x M.2 M-Key 2280 for NVMe SSD (1 x PCIe gen5 x4, 1 x PCIe gen4 x4) (option by SKU)

1.3.2 Memory

- **RAM:** 4 x 288-pin UDIMMs/CUDIMMs socket support dual channel DDR5 5600MT/s UDIMMs/CUDIMMs, up to 192GB Max.

1.3.3 Input/Output

- **Serial ports:** 6 serial ports (5 x RS-232, COM 2 RS-232/422/485 with auto flow control).
- **USB port:** Supports 1 x USB4 Gen 3x2 40Gbps Type-C, DisplayPort1.4 Alt. Mode (option by SKU), 6 x USB3.2 Gen2 Type-A, 2 x USB3.2 Gen1, 4 x USB2.0
- **GPIO connector:** 8-bit general purpose Input/Output.

1.3.4 Graphics

- **Controller:** Intel Enhanced Intel® Xe LPG architecture
- **eDP:** Supports 1 eDP max. resolution up to 4096 x 2160 @60Hz.
- **DP (via USB type C):** Supports DP 1.4 max. resolution up to 4096 x 2160 @120Hz
- **DP:** Supports 2 x DP++ 1.4 max. resolution up to 4096 x 2160 @120Hz
- **HDMI:** Supports 1 HDMI 2.1 TMDS max. resolution up to 4096 x 2160 @60Hz.

1.3.5 Ethernet LAN

- Supports dual 10/100/1000/2500 Mbps Ethernet port (s)
- **Controller:**
 - LAN1: Intel I226 2.5 GbE (I226-LM, V-PRO)
 - LAN2: Intel I226 2.5 GbE (I226-V)
 - LAN3: Intel I210 1 GbE (I210-AT)
 - LAN4: Intel I210 1 GbE (I210-AT)

1.3.6 Industrial Features

- **Watchdog timer:** Can generate a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels).

1.3.7 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 60°C (32 ~ 140°F)
- **Storage temperature:** -40 ~ 85°C (-40 ~ 185°F)
- **Humidity:** 5 ~ 95% non-condensing.
- **Power supply voltage:**

Table 1.1: Power supply voltage				
Operation	+5V	3.3V	12V	12V_8P
Configuration: Intel® Core™ Ultra 285 24-Core Processor 2.50GHz with UDIMM DDR5 4800 48GB*4pcs	4.55A	0.72A	0.04A	42.04700A
Standby (5Vsb)	3A			

- **Board size:** 244 x 244 mm (9.6 x 9.6").
- **Board weight:** 1.5 kg

1.4 Jumpers and Connectors

Connectors on the AIMB-589 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure the system for your application.

Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

1.5 Board Layout: Jumper and Connector Locations

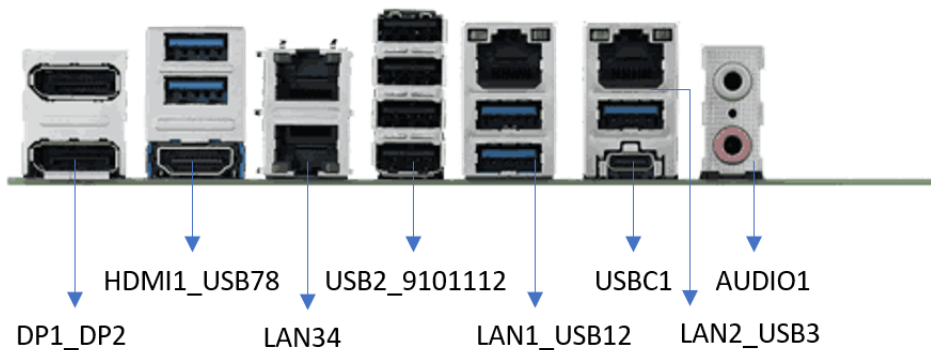


Figure 1.1 Rear I/O

Table 1.2: I/O Connector

Item	Description	Part Reference
1	Dual DisplayPort	DP1_DP2
2	High Definition Multimedia Interface+USB3.1	HDMI_USB78
3	RJ-45 2 ports	LAN34
4	USB2.0 4 ports	USB9101112
5	RJ-45 1 port + USB3.1 2 ports	LAN1_USB12
6	TBT4 / USB4.0 Type-C connector	USBC1
7	RJ-45 1 port + USB3.1 1 port	LAN2_USB3
8	HD Audio Interface	AUDIO1

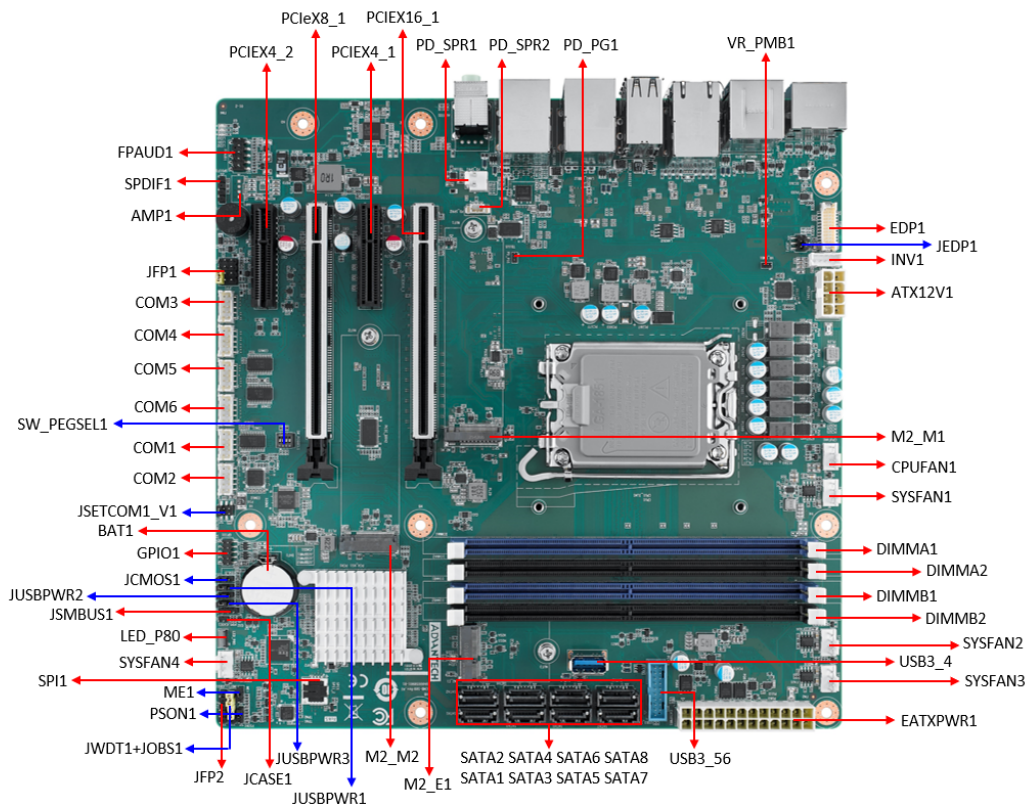


Figure 1.2 Jumper and Connector Locations (Top Side)

Table 1.3: Connector/Header List

Item	Description	Part Reference
1	100W PD module power connector	PD_SPR1
2	100W PD module signal connector	PD_SPR2
3	PD Programming Header	PD_PG1
4	PCI Express x16 slot 1	PCIEX16_1
5	PCI Express x4 slot 1	PCIEX4_1
6	PCI Express x16 slot 2 (X8 signal)	PCIeX8_1
7	PCI Express x4 slot 2	PCIEX4_2
8	Front panel audio pin header	FPAUD1
9	HD Audio interface	SPDIF1
10	Audio amplifier output pin header	AMP1
11	PWRBTN#/HDD LED/SMBUS/Speaker Header	JFP1
12	COM3 Connector	COM3
13	COM4 Connector	COM4
14	COM5 Connector	COM5
15	COM6 Connector	COM6
16	COM1 Connector	COM1
17	COM2 Connector	COM2
18	COM1 RI# selection pin header	JSETCOM1_V1
19	8-bits General Purpose I/O pin header	GPIO1
20	CMOS Clear	JCMOS1
21	USB VBUS Power Select Jump #1	JUSBPWR1
22	USB VBUS Power Select Jump #2	JUSBPWR2
23	USB VBUS Power Select Jump #3	JUSBPWR3
24	IT5782VG Programming Header	JSMBUS1
25	Case Open connector	JCASE1
26	LED port 80 connector	LED_P80
27	System Fan #4 Connector	SYSFAN4
28	Power LED and keyboard lock pin header	JFP2
29	Watchdog timer output and OBS beep	JWDT1+JOBS1
30	AT / ATX Mode selection	PSON1
31	Flash Descriptor Security Override Pin Header	ME1
32	SPI BIOS flash socket	SPI1
33	CMOS battery Connector	BAT1
34	M.2 M-Key Connector #2	M2_M2
35	PCI Express x16 Bifurcation	SW_PEGSEL1
36	M.2 M-Key Connector #1	M2_M1
37	M.2 E-Key Connector	M2_E1
38	Serial ATA interface Connector #1	SATA1
39	Serial ATA interface Connector #2	SATA2
40	Serial ATA interface Connector #3	SATA3
41	Serial ATA interface Connector #4	SATA4
42	Serial ATA interface Connector #5	SATA5
43	Serial ATA interface Connector #6	SATA6
44	USB 3.2 Gen2 Connector	USB3_4
45	Serial ATA interface Connector #7	SATA7

Table 1.3: Connector/Header List

46	Serial ATA interface Connector #8	SATA8
47	USB 3.2 GEN1 Connector	USB3_56
48	ATX 24pin power connector	EATXPWR1
49	System Fan #3 Connector	SYSFAN3
50	System Fan #2 Connector	SYSFAN2
51	DDR5 U-DIMM socket B2	DIMMB2
52	DDR5 U-DIMM socket B1	DIMMB1
53	DDR5 U-DIMM socket A2	DIMMA2
54	DDR5 U-DIMM socket A1	DIMMA1
55	System Fan #1 Connector	SYSFAN1
56	CPU FAN #1 Connector	CPUFAN1
57	ATX 8pin power connector	ATX12V1
58	EDP Backlight Inverter Power Connector	INV1
59	EDP connector	EDP1
60	EDP Panel Voltage Selection	JEDP1
61	IMVP9.2 VR Programming Header	VR_PMB1

1.6 AIMB-589 Board Diagram

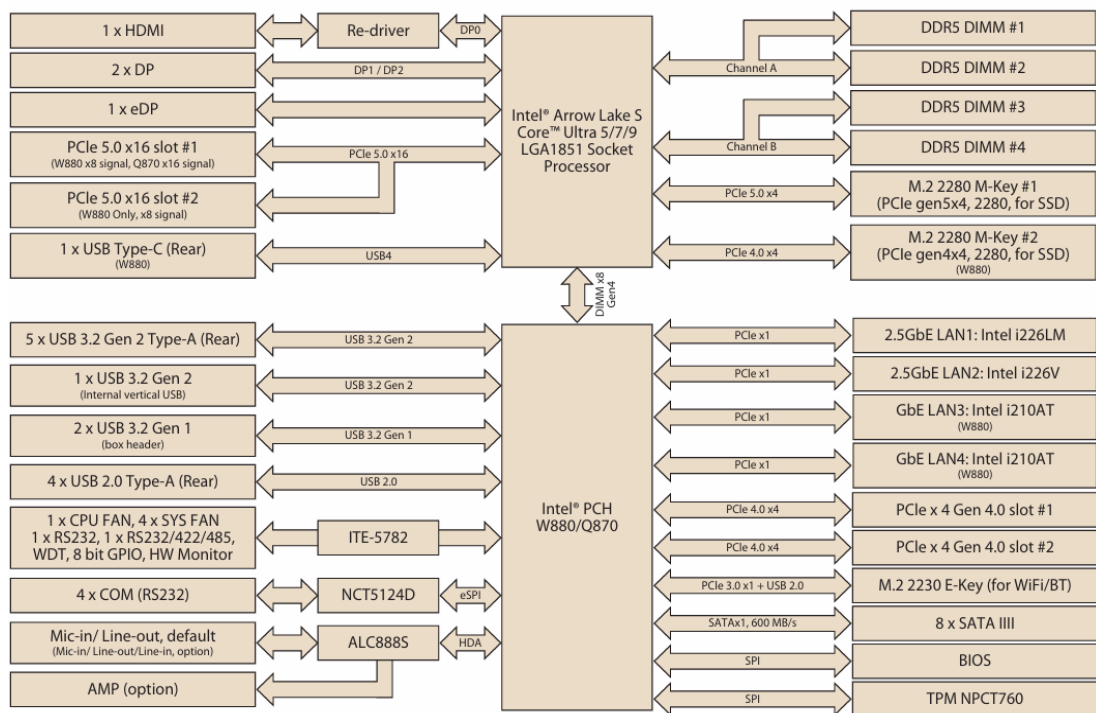


Figure 1.3 AIMB-589 Board Diagram

1.7 Safety Precautions

Warning! *Always completely disconnect the power cord from chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.*



Caution! *Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.*



Caution! *The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if battery is incorrectly replaced. Replace only with same or equivalent type recommended by the manufacturer. Discard used batteries according to manufacturer's instructions.*



Caution! *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*



1.8 Jumper Settings

This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboard's default settings and your options for each jumper.

1.8.1 How to Set Jumpers

You can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” (or turn ON) a jumper, you connect the pins with the clip. To “open” (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case, you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

1.8.2 COM1 RI# Selection Pin Header (JSETCOM1_V1)

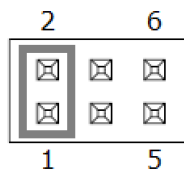


Table 1.4:

Pin	Signal	Pin	Signal
1	RI# [1]	2	Advantech define
3	Advantech define	4	+5V
5	+12V	6	Advantech define

Table 1.5:

Function	Jumper Setting
Jumper position for RI# (Default)	
Jumper position for +5V	
Jumper position for +12V	

1.8.3 CMOS Clear (JCMOS1)



Table 1.6:

Pin	Signal
1	NC
3	RTC_RESET#
5	GND

Table 1.7:

Function	Jumper Setting
Normal (Default) JCMOS1(1-2)	<p>Diagram showing a 3-pin header with pins 1, 2, and 3. Pins 1 and 2 are connected by a dark grey jumper, while pin 3 is open.</p>
Clear CMOS JCMOS1(2-3)	<p>Diagram showing a 3-pin header with pins 1, 2, and 3. Pins 2 and 3 are connected by a dark grey jumper, while pin 1 is open.</p>

1.8.4 USB VBUS Power Select Jump #1 (JUSBPWR1/JUSBPWR2/JUSBPWR3)



Table 1.8:

Pin	Signal
1	+5V _{SB}
3	Advantech Define
5	+5V

Table 1.9:

Function	Jumper Settings
USB power up at S5 (Default)	
USB power up at S0	

1.8.5 Watchdog Timer Output and OBS Beep (JWDT1+JOBS1)



Table 1.10:

Pin	Signal
1	NC
2	Watch Dog Reset# output
3	System Reset input#
4	SIO Warning Beep output
5	SP1 Buzzer Beep input

Table 1.11:

Function	Jumper Settings
Watchdog Timer Output(2-3) (Default) OBS BEEP(4-5) (Default)	
Watchdog Timer Disable(1-2) OBS BEEP(4-5) (Default)	

1.8.6 AT/ATX Mode Selection (PSON1)

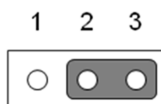


Table 1.12:

Pin	Signal
1	AT
2	+3.3V
3	ATX

Table 1.13:

Function	Jumper Settings
ATX Mode (Default) PSON1(2-3)	1 2 3
AT Mode PSON1(1-2)	1 2 3

1.8.7 Flash Descriptor Security Override Pin Header (ME1)



Table 1.14:

Pin	Signal
1	Advantech Define
2	Advantech Define
3	NC

Table 1.15:

Function	Jumper Settings
Disable Flash Descriptor Security (Default)	1 2 3
Enable Flash Descriptor Security	1 2 3

1.8.8 PCI Express x16 Bifurcation (SW_PEGSEL1)

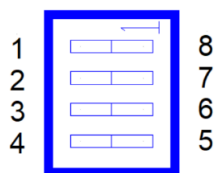


Table 1.16:

Pin	Signal
1	PEG0CFGSEL [1]
2	PEG0CFGSEL [0]
3	Advantech define
4	NC

Table 1.17:

Function	Jumper Settings
1 X16 (Q870 Default)	
2 X8 (W880 Default)	
1 X8 + 2 X4	

1.8.9 EDP Panel Voltage Selection (JEDP1)

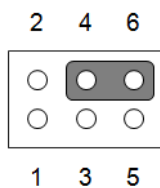


Table 1.18:

Pin	Signal	Pin	Signal
1	NC	2	+5V
3	+12V	4	VDD
5	NC	6	+3.3V

Table 1.19:

Function	Jumper Settings
Jumper position for 5V	
Jumper position for 3.3V (Default)	
Jumper position for 12V	

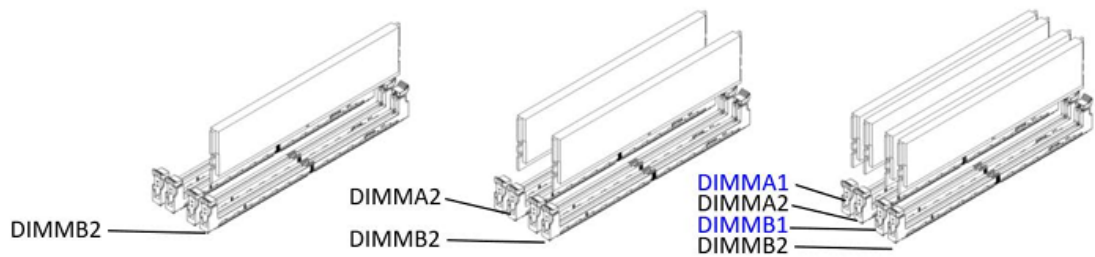
1.9 System Memory

The AIMB-589 has four 288-pin DDR5 memory sockets for modules with maximum capacity of 192GB (maximum 48GB for each DIMM). The AIMB-589QM supports only non-ECC DDR5 memory modules, and can support ECC/non-ECC DDR5 memory modules.

1.10 Memory Installation Procedures

To install DIMMs, first make sure the two handles of the DIMM socket are in the “open” position, i.e., the handles lean outward. Slowly slide the DIMM module along the plastic guides on both ends of the socket. Then firmly but gently (avoid pushing down too hard) press the DIMM module well down into the socket, until you hear a click when the two handles have automatically locked the memory module into the correct position of the DIMM socket. To remove the memory module, just push both handles outward, and the memory module will be ejected by the mechanism.

- DIMM installation It is recommended that you use the same UDIMM memory module on the same channel and load the module from the 2nd slot if a single module is used, as shown in the picture below.



Chapter 2

Connecting
Peripherals

2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

2.2 I/O Connector

2.2.1 Dual DisplayPort Stack up Connector (DP1_DP2)

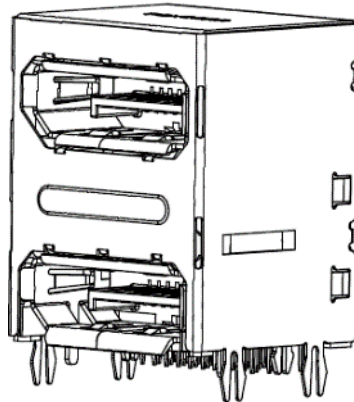


Table 2.1: Dual DisplayPort Stack up Connector (DP1_DP2)

Pin	Signal	Pin	Signal
P1	DP1_0+	P21	DP2_0+
P2	GND	P22	GND
P3	DP1_0-	P23	DP2_0-
P4	DP1_1+	P24	DP2_1+
P5	GND	P25	GND
P6	DP1_1-	P26	DP2_1-
P7	DP1_2+	P27	DP2_2+
P8	GND	P28	GND
P9	DP1_2-	P29	DP2_2-
P10	DP1_3+	P30	DP2_3+
P11	GND	P31	GND
P12	DP1_3-	P32	DP2_3-
P13	DP1_AUX_EN#	P33	DP2_AUX_EN#
P14	GND	P34	GND
P15	DP1_AUX+	P35	DP2_AUX+
P16	GND	P36	GND
P17	DP1_AUX-	P37	DP2_AUX-
P18	DP1_HPD	P38	DP2_HPD
P19	GND	P39	GND
P20	+V3.3_DP1	P40	+V3.3_DP1

2.2.2 High-Definition Multimedia Interface + USB3.2 Gen2 (HDMI1_USB78)

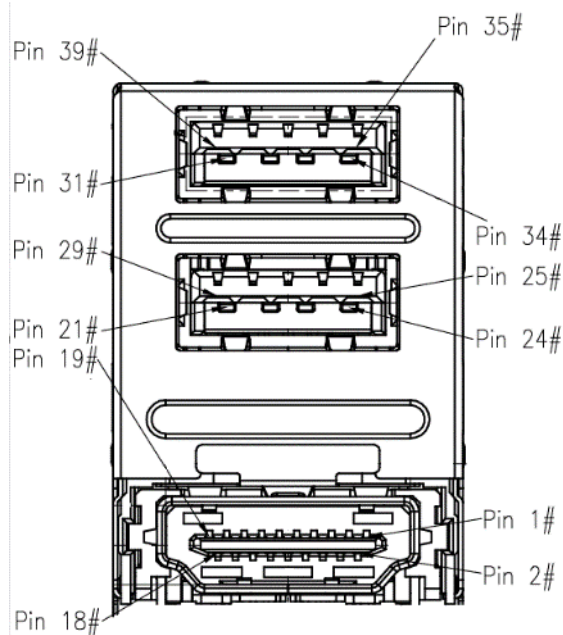


Table 2.2: High-Definition Multimedia Interface + USB3.2 Gen2 (HDMI1_USB78)

Pin	Signal	Pin	Signal
1	HDMI1_z_D2+	21	VBUS
2	GND	22	D7-
3	HDMI1_z_D2-	23	D7+
4	HDMI1_z_D1+	24	GND
5	GND	25	RX7-
6	HDMI1_z_D1-	26	RX7+
7	HDMI1_z_D0+	27	GND
8	GND	28	TX7-
9	HDMI1_z_D0-	29	TX7+
10	HDMI1_z_CLK+		
11	GND	31	VBUS
12	HDMI1_z_CLK-	32	D8-
13	NC	33	D8+
14	NC	34	GND
15	HDMI1_SCL	35	RX8-
16	HDMI1_SDA	36	RX8+
17	GND	37	GND
18	+V5_HDMI1	38	TX8-
19	HDMI1_HPD	39	TX8+

2.2.3 RJ-45 Stack up Connector (LAN34)

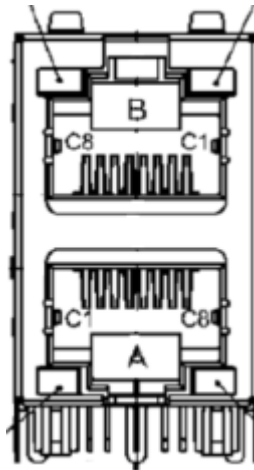


Table 2.3: RJ-45 Stack up Connector (LAN34)

Pin	Signal	Pin	Signal
C1 (A)	TX1+	C1 (B)	TX1+
C2 (A)	TX1-	C2 (B)	TX1-
C3 (A)	TX2+	C3 (B)	TX2+
C4 (A)	TX3+	C4 (B)	TX3+
C5 (A)	TX3-	C5 (B)	TX3-
C6 (A)	TX2-	C6 (B)	TX2-
C7 (A)	TX4+	C7 (B)	TX4+
C8 (A)	TX4-	C8 (B)	TX4-

2.2.4 Universal Serial Bus 2.0 Port 9, 10, 11, 12 (USB2_9101112)

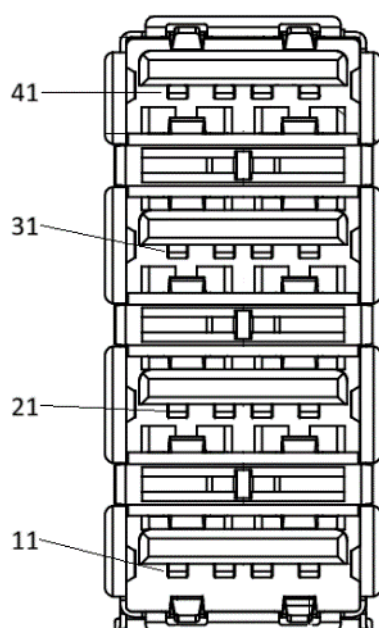


Table 2.4: Universal Serial Bus 2.0 Port 9, 10, 11, 12 (USB2_9101112)

Pin	Signal
11	VBUS
12	D9-
13	D9+
14	GND
21	VBUS
22	D10-
23	D10+
24	GND
31	VBUS
32	D11-
33	D11+
34	GND
41	VBUS
42	D12-
43	D12+
44	GND

2.2.5 RJ-45 + USB3.2 Stack Connector (LAN1_USB12)

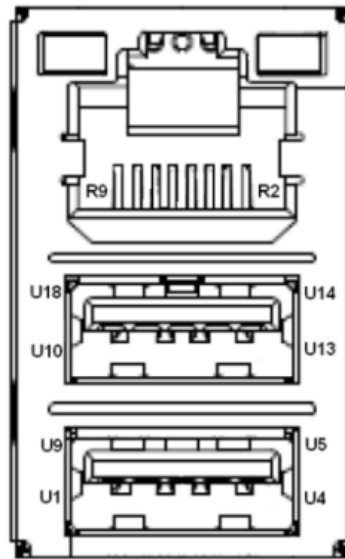


Table 2.5:

Pin	Signal	Pin	Signal
U1	VBUS	U10	VBUS
U2	D1-	U11	D2-
U3	D1+	U12	D2+
U4	GND	U13	GND
U5	RX1-	U14	RX2-
U6	RX1+	U15	RX2+
U7	GND	U16	GND
U8	TX1-	U17	TX2-
U9	TX1+	U18	TX2+

Table 2.6:

Pin	Signal	Pin	Signal
R2	TX1+	R6	TX3
R3	TX1-	R7	TX2-
R4	TX2+	R8	TX4+
R5	TX3+	R9	TX4-

2.2.6 TBT4/USB4.0 Type-C Connector (USBC1)

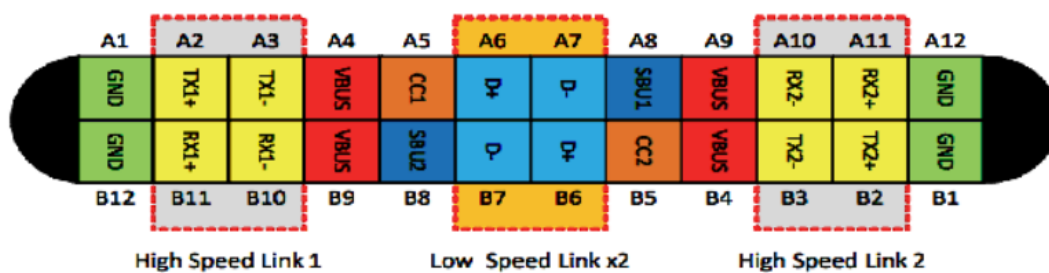


Table 2.7: TBT4/USB4.0 Type-C Connector (USBC1)

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	SS_TX1+	B2	SS_TX2+
A3	SS_TX1-	B3	SS_TX2-
A4	VUSB	B4	VUSB
A5	CC1	B5	CC2
A6	D1+	B6	D2+
A7	D1-	B7	D2-
A8	SBU1	B8	SBU2
A9	VUSB	B9	VUSB
A10	SS_RX2-	B10	SS_RX1-
A11	SS_RX2+	B11	SS_RX1+
A12	GND	B12	GND

2.2.7 RJ-45 + USB3.2 (LAN2_USB3)

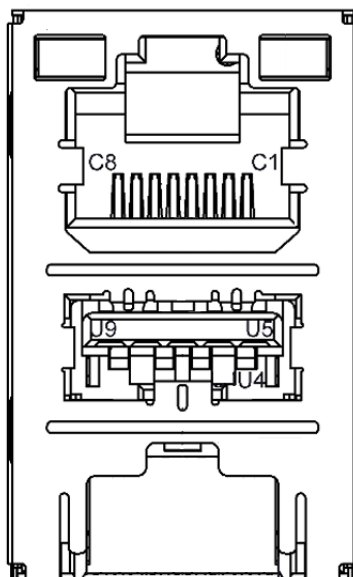


Table 2.8:

Pin	Signal
U1	VBUS
U2	D3-
U3	D3+
U4	GND
U5	RX3-
U6	RX3+
U7	GND
U8	TX3-
U9	TX3+

Table 2.9:

Pin	Signal	Pin	Signal
C1	TX1+	C5	TX3-
C2	TX1-	C6	TX2-
C3	TX2+	C7	TX4+
C4	TX3+	C8	TX4-

2.2.8 HD Audio Interface (AUDIO1)

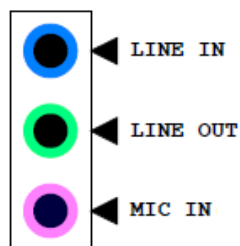


Table 2.10: HD Audio Interface (AUDIO1)

Pin	Signal
1	MIC IN
2	LINE OUT
3	LINE IN

2.2.9 100W PD Module Power Connector (PD_SPR1)

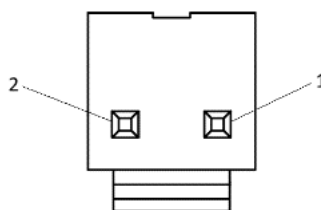


Table 2.11: 100W PD Module Power Connector (PD_SPR1)

Pin	Signal
1	CHGR_VIN
2	GND

2.2.10 100W PD Module Signal Connector (PD_SPR2)

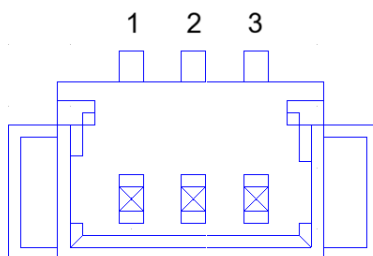


Table 2.12: 100W PD Module Signal Connector (PD_SPR2)

Pin	Signal
1	SCL
2	SDA
3	DETECT#

2.2.11 PD Programming Header (PD_PG1)



Table 2.13: PD Programming Header (PD_PG1)

Pin	Signal
1	SCL
2	SDA
3	GND

2.2.12 PCI-Express x16 Slot 1 (PCIEX16_1)

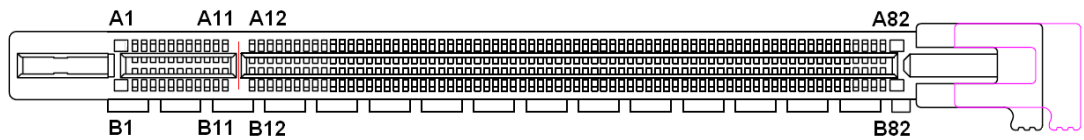


Table 2.14: PCI-Express x16 Slot 1 (PCIEX16_1)

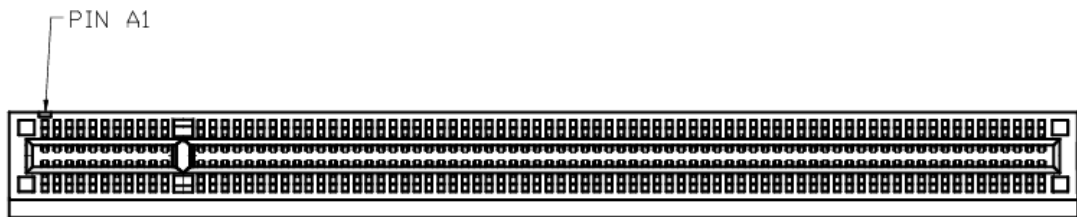
Pin	Signal	Pin	Signal
B1	+12V	A1	GND
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	RSVD
B6	SMB_DAT	A6	RSVD
B7	GND	A7	RSVD
B8	+3.3V	A8	RSVD
B9	RSVD	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	PE_WAKE#	A11	PERST#
B12	CLK_REQ#	A12	GND
B13	GND	A13	REFCLK+
B14	TX0+	A14	REFCLK-
B15	TX0-	A15	GND
B16	GND	A16	RX0+
B17	RSVD	A17	RX0-
B18	Advantech Define	A18	GND
B19	TX1+	A19	Advantech define
B20	TX1-	A20	GND
B21	GND	A21	RX1+
B22	GND	A22	RX1-
B23	TX2+	A23	GND
B24	TX2-	A24	GND
B25	GND	A25	RX2+

B26	GND	A26	RX2-
B27	TX3+	A27	GND
B28	TX3-	A28	GND
B29	GND	A29	RX3+
B30	RSVD	A30	RX3-
B31	RSVD	A31	GND
B32	GND	A32	Advantech define
B33	TX4+	A33	NC
B34	TX4-	A34	GND
B35	GND	A35	RX4+
B36	GND	A36	RX4-
B37	TX5+	A37	GND
B38	TX5-	A38	GND
B39	GND	A39	RX5+
B40	GND	A40	RX5-
B41	TX6+	A41	GND
B42	TX6-	A42	GND
B43	GND	A43	RX6+
B44	GND	A44	RX6-
B45	TX7+	A45	GND
B46	TX7-	A46	GND
B47	GND	A47	RX7+
B48	RSVD	A48	RX7-
B49	GND	A49	GND
B50	TX8+	A50	NC
B51	TX8-	A51	GND
B52	GND	A52	RX8+
B53	GND	A53	RX8-
B54	TX9+	A54	GND
B55	TX9-	A55	GND
B56	GND	A56	RX9+
B57	GND	A57	RX9-
B58	TX10+	A58	GND
B59	TX10-	A59	GND
B60	GND	A60	RX10+
B61	GND	A61	RX10-
B62	TX11+	A62	GND
B63	TX11-	A63	GND
B64	GND	A64	RX11+
B65	GND	A65	RX11-
B66	TX12+	A66	GND
B67	TX12-	A67	GND
B68	GND	A68	RX12+
B69	GND	A69	RX12-
B70	TX13+	A70	GND
B71	TX13-	A71	GND
B72	GND	A72	RX13+

Table 2.14: PCI-Express x16 Slot 1 (PCIEX16_1)

B73	GND	A73	RX13-
B74	TX14+	A74	GND
B75	TX14-	A75	GND
B76	GND	A76	RX14+
B77	GND	A77	RX14-
B78	TX15+	A78	GND
B79	TX15-	A79	GND
B80	GND	A80	RX15+
B81	RSVD	A81	RX15-
B82	NC	A82	GND

2.2.13 PCI Express x4 Slot 1 (PCIEX4_1)

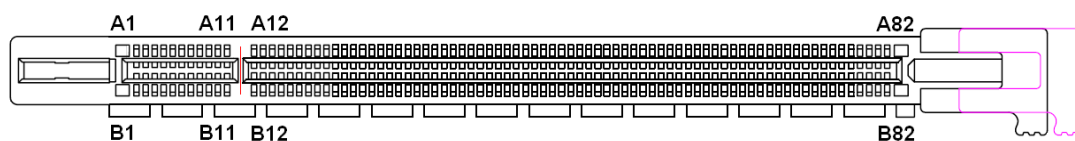
**Table 2.15: PCI Express x4 Slot 1 (PCIEX4_1)**

Pin	Signal	Pin	Signal
B1	+12V	A1	GND
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	RSVD
B6	SMB_DAT	A6	RSVD
B7	GND	A7	NC
B8	+3.3V	A8	RSVD
B9	RSVD	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	PE_WAKE#	A11	PERST#
B12	CLK_REQ#	A12	GND
B13	GND	A13	REFCLK+
B14	TX0+	A14	REFCLK-
B15	TX0-	A15	GND
B16	GND	A16	RX0+
B17	RSVD	A17	RX0-
B18	GND	A18	GND
B19	TX1+	A19	NC
B20	TX1-	A20	GND
B21	GND	A21	RX1+
B22	GND	A22	RX1-
B23	TX2+	A23	GND
B24	TX2-	A24	GND

Table 2.15: PCI Express x4 Slot 1 (PCIEX4_1)

B25	GND	A25	RX2+
B26	GND	A26	RX2-
B27	TX3+	A27	GND
B28	TX3-	A28	GND
B29	GND	A29	RX3+
B30	Reserved	A30	RX3-
B31	Reserved	A31	GND
B32	GND	A32	NC

2.2.14 PCI Express x16 Slot 2 (X8 signal) (PCIEX8_1)

**Table 2.16: PCI Express x16 Slot 2 (X8 signal) (PCIEX8_1)**

Pin	Signal	Pin	Signal
B1	+12V	A1	GND
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	RSVD
B6	SMB_DAT	A6	RSVD
B7	GND	A7	NC
B8	+3.3V	A8	RSVD
B9	RSVD	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	PE_WAKE#	A11	PERST#
B12	CLK_REQ#	A12	GND
B13	GND	A13	REFCLK+
B14	TX0+	A14	REFCLK-
B15	TX0-	A15	GND
B16	GND	A16	RX0+
B17	RSVD	A17	RX0-
B18	GND	A18	GND
B19	TX1+	A19	Advantech define
B20	TX1-	A20	GND
B21	GND	A21	RX1+
B22	GND	A22	RX1-
B23	TX2+	A23	GND
B24	TX2-	A24	GND
B25	GND	A25	RX2+
B26	GND	A26	RX2-
B27	TX3+	A27	GND
B28	TX3-	A28	GND

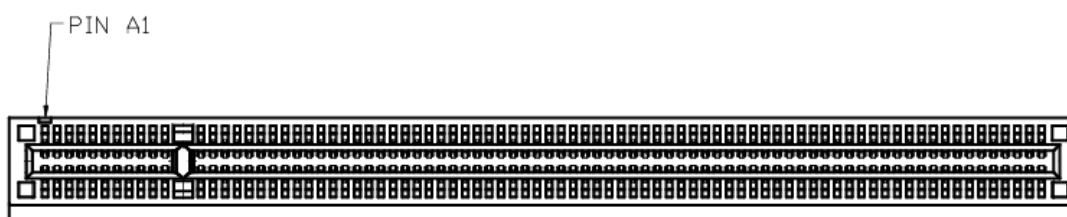
Table 2.16: PCI Express x16 Slot 2 (X8 signal) (PCIEX8_1)

B29	GND	A29	RX3+
B30	RSVD	A30	RX3-
B31	RSVD	A31	GND
B32	GND	A32	Advantech define
B33	TX4+	A33	RSVD
B34	TX4-	A34	GND
B35	GND	A35	RX4+
B36	GND	A36	RX4-
B37	TX5+	A37	GND
B38	TX5-	A38	GND
B39	GND	A39	RX5+
B40	GND	A40	RX5-
B41	TX6+	A41	GND
B42	TX6-	A42	GND
B43	GND	A43	RX6+
B44	GND	A44	RX6-
B45	TX7+	A45	GND
B46	TX7-	A46	GND
B47	GND	A47	RX7+
B48	RSVD	A48	RX7-
B49	GND	A49	GND
B50	NC	A50	RSVD
B51	NC	A51	GND
B52	GND	A52	NC
B53	GND	A53	NC
B54	NC	A54	GND
B55	NC	A55	GND
B56	GND	A56	NC
B57	GND	A57	NC
B58	NC	A58	GND
B59	NC	A59	GND
B60	GND	A60	NC
B61	GND	A61	NC
B62	NC	A62	GND
B63	NC	A63	GND
B64	GND	A64	NC
B65	GND	A65	NC
B66	NC	A66	GND
B67	NC	A67	GND
B68	GND	A68	NC
B69	GND	A69	NC
B70	NC	A70	GND
B71	NC	A71	GND
B72	GND	A72	NC
B73	GND	A73	NC
B74	NC	A74	GND
B75	NC	A75	GND

Table 2.16: PCI Express x16 Slot 2 (X8 signal) (PCIEX8_1)

B76	GND	A76	NC
B77	GND	A77	NC
B78	NC	A78	GND
B79	NC	A79	GND
B80	GND	A80	NC
B81	RSVD	A81	NC
B82	RSVD	A82	GND

2.2.15 PCI Express x4 Slot 2 (PCIEX4_2)

**Table 2.17: PCI Express x4 Slot 2 (PCIEX4_2)**

Pin	Signal	Pin	Signal
B1	+12V	A1	GND
B2	+12V	A2	+12V
B3	+12V	A3	+12V
B4	GND	A4	GND
B5	SMB_CLK	A5	RSVD
B6	SMB_DAT	A6	RSVD
B7	GND	A7	NC
B8	+3.3V	A8	RSVD
B9	RSVD	A9	+3.3V
B10	+3.3VAUX	A10	+3.3V
B11	PE_WAKE#	A11	PERST#
B12	CLK_REQ#	A12	GND
B13	GND	A13	REFCLK+
B14	TX0+	A14	REFCLK-
B15	TX0-	A15	GND
B16	GND	A16	RX0+
B17	RSVD	A17	RX0-
B18	GND	A18	GND
B19	TX1+	A19	NC
B20	TX1-	A20	GND
B21	GND	A21	RX1+
B22	GND	A22	RX1-
B23	TX2+	A23	GND
B24	TX2-	A24	GND
B25	GND	A25	RX2+
B26	GND	A26	RX2-
B27	TX3+	A27	GND

Table 2.17: PCI Express x4 Slot 2 (PCIEX4_2)

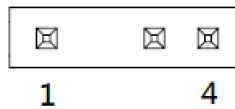
B28	TX3-	A28	GND
B29	GND	A29	RX3+
B30	Reserved	A30	RX3-
B31	Reserved	A31	GND
B32	GND	A32	NC

2.2.16 Front Panel Audio Pin Header (FPAUD1)

**Table 2.18: Front Panel Audio Pin Header (FPAUD1)**

Pin	Signal	Pin	Signal
1	MIC IN-L	2	GND
3	MIC IN-R	4	FPAUD_DETECT#
5	LINE OUT-R	6	SENSE R1
7	SENSE	8	KEY
9	LINE OUT-L	10	SENSE R2

2.2.17 HD Audio Interface (SPDIF1)

**Table 2.19: HD Audio Interface (SPDIF1)**

Pin	Signal
1	+5V
2	KEY
3	SPDIF OUT
4	GND

2.2.18 Audio Amplifier Output Pin Header (AMP1)

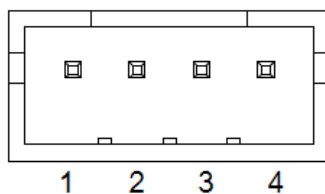


Table 2.20: Audio Amplifier Output Pin Header (AMP1)

Pin	Signal
1	AMP OUT – R+
2	AMP OUT – R-
3	AMP OUT – L-
4	AMP OUT – L+

2.2.19 PWRBTN#/HDD LED/SMBUS/Speaker Header (JFP1)

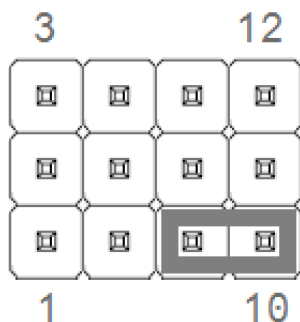


Table 2.21: PWRBTN#/HDD LED/SMBUS/Speaker Header (JFP1)

Pin	Signal	Pin	Signal
1	+5V	2	HDD LED+
3	Power Button+	4	SPK_P2
5	HDD LED-	6	Power Button-
7	SPK_P3	8	SMB_DATA
9	System Reset+	10	SPK_P4
11	SMB_CLK	12	System Reset-

2.2.20 COM3 Connector (COM3)

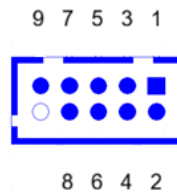


Table 2.22: COM3 Connector (COM3)

Pin	Signal	Pin	Signal
1	COM3_DCD#	2	COM3_SIN
3	COM3_SOUT	4	COM3_DTR#
5	GND	6	COM3_DSR#
7	COM3_RTS#	8	COM3_CTS#
9	COM3_RI#		

2.2.21 COM4 Connector (COM4)

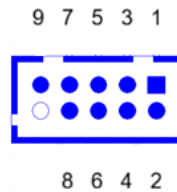


Table 2.23: COM4 Connector (COM4)

Pin	Signal	Pin	Signal
1	COM4_DCD#	2	COM4_SIN
3	COM4_SOUT	4	COM4_DTR#
5	GND	6	COM4_DSR#
7	COM4_RTS#	8	COM4_CTS#
9	COM4_RI#		

2.2.22 COM5 Connector (COM5)

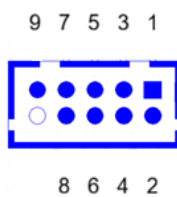


Table 2.24: COM5 Connector (COM5)

Pin	Signal	Pin	Signal
1	COM5_DCD#	2	COM5_SIN
3	COM5_SOUT	4	COM5_DTR#
5	GND	6	COM5_DSR#
7	COM5_RTS#	8	COM5_CTS#
9	COM5_RI#		

2.2.23 COM6 Connector (COM6)

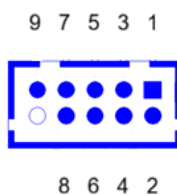


Table 2.25: COM6 Connector (COM6)

Pin	Signal	Pin	Signal
1	COM6_DCD#	2	COM6_SIN
3	COM6_SOUT	4	COM6_DTR#
5	GND	6	COM6_DSR#
7	COM6_RTS#	8	COM6_CTS#
9	COM6_RI#		

2.2.24 COM1 Connector (COM1)

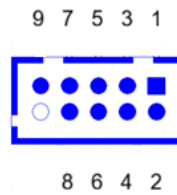


Table 2.26: COM1 Connector (COM1)

Pin	Signal	Pin	Signal
1	COM1_DCD#	2	COM1_SIN
3	COM1_SOUT	4	COM1_DTR#
5	GND	6	COM1_DSR#
7	COM1_RTS#	8	COM1_CTS#
9	COM1_RI_V#		

2.2.25 COM2 Connector (COM2)

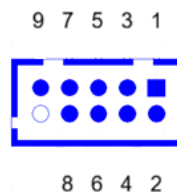


Table 2.27: COM2 Connector (COM2)

Pin	Signal	Pin	Signal
1	COM2_422_485_TX-	2	COM2_422_485_TX+
3	COM2_422_RX+	4	COM2_422_RX-
5	GND	6	COM2_DSR#
7	COM2_RTS#	8	COM2_CTS#
9	COM2_RI#		

2.2.26 8-bit General Purpose I/O Pin Header (GPIO1)

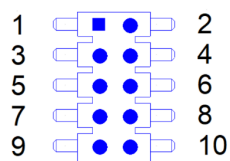


Table 2.28: 8-bit General Purpose I/O Pin Header (GPIO1)

Pin	Signal	Pin	Signal
1	GPIO1	2	GPIO4
3	GPIO2	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	VCC_GPIO	10	GND

2.2.27 IT5782VG Programming Header (JSMBUS1)

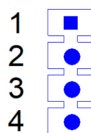


Table 2.29: IT5782VG Programming Header (JSMBUS1)

Pin	Signal
1	+V3.3_A_SIO
2	SMB_CLK_EC
3	SMB_DAT_EC
4	GND

2.2.28 Case Open Connector (JCASE1)

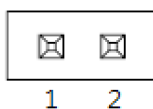


Table 2.30: Case Open connector (JCASE1)

Pin	Signal
1	Case Open
2	GND

2.2.29 LED Port 80 Connector (LED_P80)

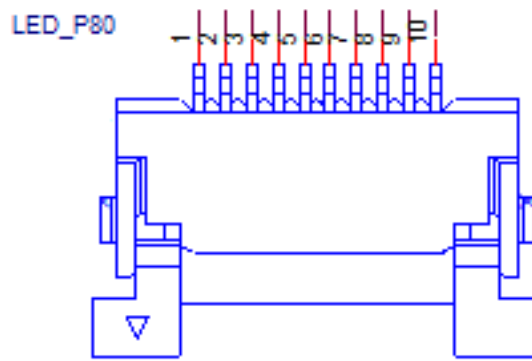


Table 2.31: LED Port 80 Connector (LED_P80)

Pin	Signal
1	GND
2	LED_A
3	LED_B
4	LED_C
5	LED_D
6	LED_E
7	LED_F
8	LED_G
9	DGH0#
10	DGL0#

2.2.30 Power LED and Keyboard Lock Pin Header (JFP2)



Table 2.32: Power LED and Keyboard Lock Pin Header (JFP2)

Pin	Signal
1	SIO_SUSLED+
2	NC
3	SIO_SUSLED-
4	NC
5	GND

2.2.31 SPI BIOS Flash Socket1 (SPI1)

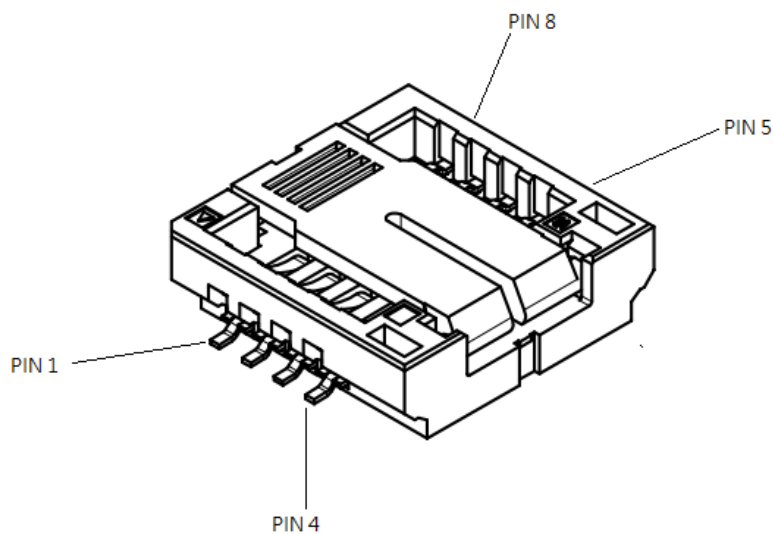


Table 2.33: SPI BIOS Flash Socket1 (SPI1)

Pin	Signal	Pin	Signal
1	CS#	5	MOSI
2	MISO	6	SCLK
3	WP# / IO2	7	HOLD# / IO3
4	GND	8	+V3.3_SPI

2.2.32 CMOS Battery Connector (BAT1)

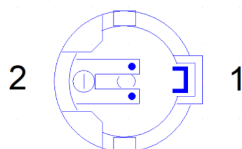


Table 2.34: CMOS Battery Connector (BAT1)

Pin	Signal
1	+VBAT
2	GND

2.2.33 M.2 M-Key Connector #2 (M2_M2)

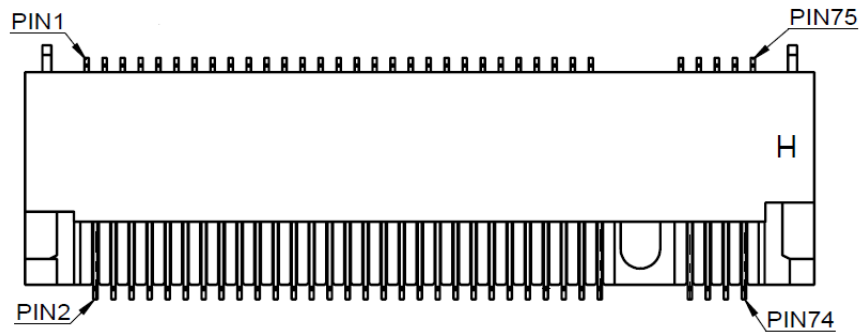


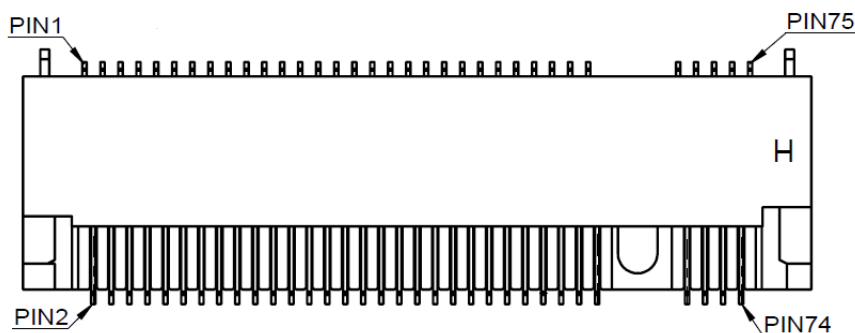
Table 2.35: M.2 M-Key Connector #2 (M2_M2)

Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	GND	4	3.3V
5	PERn3	6	N/C
7	PERp3	8	N/C
9	GND	10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)
11	PETn3	12	3.3V
13	PETp3	14	3.3V
15	GND	16	3.3V
17	PERn2	18	3.3V
19	PERp2	20	N/C
21	GND	22	N/C
23	PETn2	24	N/C
25	PETp2	26	N/C
27	GND	28	N/C
29	PERn1	30	N/C
31	PERp1	32	N/C
33	GND	34	N/C
35	PETn1	36	N/C
37	PETp1	38	DEVSLP (O)
39	GND	40	N/C
41	PERn0/SATA-B+	42	N/C
43	PERp0/SATA-B-	44	N/C
45	GND	46	N/C
47	PETn0/SATA-A-	48	N/C
49	PETp0/SATA-A+	50	PERST# (O)(0/3.3V) or N/C
51	GND	52	CLKREQ# (I/O)(0/3.3V) or N/C
53	REFCLKn	54	PEWAKE# (I/O)(0/3.3V) or N/C
55	REFCLKp	56	N/C
57	GND	58	N/C
59	Connector Key	60	Connector Key
61	Connector Key	62	Connector Key
63	Connector Key	64	Connector Key
65	Connector Key	66	Connector Key

Table 2.35: M.2 M-Key Connector #2 (M2_M2)

67	N/C	68	SUSCLK(32kHz) (O)(0/3.3V)
69	PEDET (NC-PCIe/GND-SATA)	70	3.3V
71	GND	72	3.3V
73	GND	74	3.3V
75	GND		

2.2.34 M.2 M-KEY Connector #1 (M2_M1)

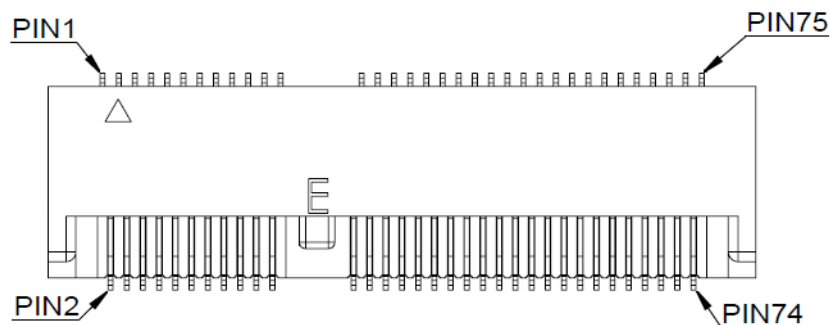
**Table 2.36: M.2 M-Key Connector #1 (M2_M1)**

Pin	Signal	Pin	Signal
1	GND	2	3.3V
3	GND	4	3.3V
5	PERn3	6	N/C
7	PERp3	8	N/C
9	GND	10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)
11	PETn3	12	3.3V
13	PETp3	14	3.3V
15	GND	16	3.3V
17	PERn2	18	3.3V
19	PERp2	20	N/C
21	GND	22	N/C
23	PETn2	24	N/C
25	PETp2	26	N/C
27	GND	28	N/C
29	PERn1	30	N/C
31	PERp1	32	N/C
33	GND	34	N/C
35	PETn1	36	N/C
37	PETp1	38	DEVSLP (O)
39	GND	40	N/C
41	PERn0/SATA-B+	42	N/C
43	PERp0/SATA-B-	44	N/C
45	GND	46	N/C
47	PETn0/SATA-A-	48	N/C
49	PETp0/SATA-A+	50	PERST# (O)(0/3.3V) or N/C

Table 2.36: M.2 M-Key Connector #1 (M2_M1)

51	GND	52	CLKREQ# (I/O)(0/3.3V) or N/C
53	REFCLKn	54	PEWAKE# (I/O)(0/3.3V) or N/C
55	REFCLKp	56	N/C
57	GND	58	N/C
59	Connector Key	60	Connector Key
61	Connector Key	62	Connector Key
63	Connector Key	64	Connector Key
65	Connector Key	66	Connector Key
67	N/C	68	SUSCLK(32kHz) (O)(0/3.3V)
69	PEDET (NC-PCIe/GND-SATA)	70	3.3V
71	GND	72	3.3V
73	GND	74	3.3V
75	GND		

2.2.35 M.2 E-Key Connector (M2_E1)

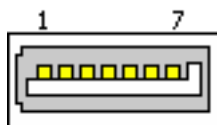
**Table 2.37: M.2 E-Key Connector (M2_E1)**

Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	USB_D+	4	+3.3V
5	USB_D-	6	WLAN_LED1#
7	GND	8	BT_PCMCLK
9	CNV_WR_D1-	10	BT_PCMFRM
11	CNV_WR_D1+	12	BT_PCMin
13	GND	14	BT_PCmOUT
15	CNV_WR_D0-	16	BT_LED#
17	CNV_WR_D0+	18	GND
19	GND	20	UART WAKE#
21	CNV_WR_CLK-	22	CNV_BRI_RSP
23	CNV_WR_CLK+	24	Connector Key
25	Connector Key	26	Connector Key
27	Connector Key	28	Connector Key
29	Connector Key	30	Connector Key
31	Connector Key	32	CNV_RGI_DT_R
33	GND	34	CNV_RGI_RSP
35	PETp0	36	CNV_BRI_DT_R

Table 2.37: M.2 E-Key Connector (M2_E1)

37	PETn0	38	CL_RST#
39	GND	40	CL_DAT
41	PERp0	42	CL_CLK
43	PERn0	44	CNV_GNSS_PA_BLANKING
45	GND	46	CNV_MFUART2_TXD
47	REFCLKp0	48	CNV_MFUART2_RXD
49	REFCLKn0	50	SUSCLK
51	GND	52	WLAN_RST#
53	CLKREQ0#	54	BT_RF_KILL#
55	PEWAKE0#	56	WIFI_RF_KILL#
57	GND	58	NC
59	CNV_WT_D1-	60	NC
67	CNV_WT_D0+	68	NC
69	GND	70	NC
71	CNV_WT_CLK-	72	+3.3V
73	CNV_WT_CLK+	74	+3.3V
75	GND		

2.2.36 Serial ATA Interface Connector #1 (SATA1/SATA2/SATA3/SATA4/SATA5/SATA6/SATA7/SATA8)

**Table 2.38: Serial ATA Interface Connector #1 (SATA1/SATA2/SATA3/SATA4/SATA5/SATA6/SATA7/SATA8)**

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

2.2.37 USB 3.2 Gen1 Connector (USB3_4)

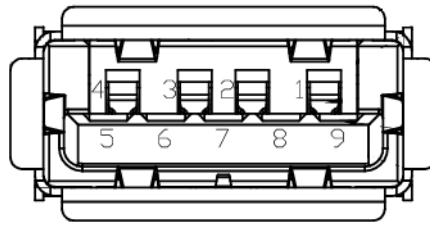


Table 2.39: USB 3.2 Gen1 Connector (USB3_4)

Pin	Signal
1	+USBV6
2	USB2_CMC_D9n
3	USB2_CMC_D9p
4	GND
5	USB32_CMC_RXN4
6	USB32_CMC_RXP4
7	GND
8	USB32_CMC_TXN4
9	USB32_CMC_TXP4

2.2.38 Universal Serial Bus 3.2 GEN1 (USB3_56)

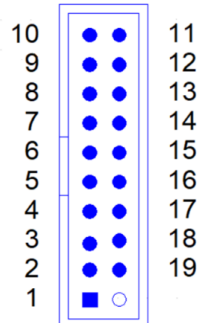


Table 2.40: Universal Serial Bus 3.2 GEN1 (USB3_56)

Pin	Signal	Pin	Signal
1	VBUS	19	VBUS
2	RX5-	18	RX6-
3	RX5+	17	RX6+
4	GND	16	GND
5	TX5-	15	TX6-
6	TX5+	14	TX6+
7	GND	13	GND
8	D5-	12	D6-
9	D5+	11	D6+
10	NC		

2.2.39 ATX 24-pin Power Connector (EATXPWR1)

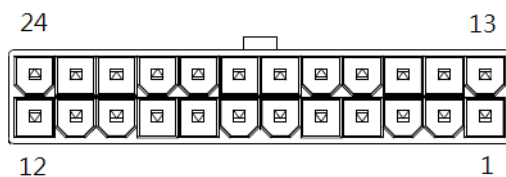


Table 2.41: ATX 24-pin Power Connector (EATXPWR1)

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PSON#
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWROK	20	-5V
9	+5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	GND

2.2.40 System Fan Connector (SYSFAN1/SYSFAN2/SYSFAN3/SYSFAN4)



Table 2.42: System Fan Connector (SYSFAN1/SYSFAN2/SYSFAN3/SYSFAN4)

Pin	Signal
1	GND
2	SYSTEM FAN VCC
3	SYSTEM FAN SPEED
4	SYSTEM FAN PWM

2.2.41 CPU Fan Connector (CPUFAN1)



Table 2.43: CPU Fan Connector (CPUFAN1)

Pin	Signal
1	GND
2	CPU FAN VCC
3	CPU FAN SPEED
4	CPU FAN PWM

2.2.42 ATX 8-pin Main Power Connector (ATX12V1)

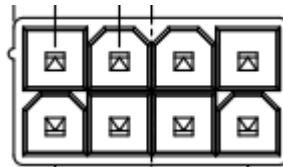


Table 2.44: ATX 8-pin Main Power Connector (ATX12V1)

Pin	Signal	Pin	Signal
1	GND	2	+12V
3	GND	4	+12V
5	GND	6	+12V
7	GND	8	+12V

2.2.43 EDP Backlight Inverter Power Connector (INV1)

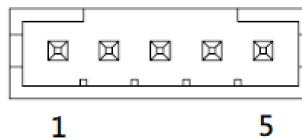


Table 2.45: EDP Backlight Inverter Power Connector (INV1)

Pin	Signal
1	+12V
2	GND
3	BKL EN
4	BKL CTRL
5	+5V

2.2.44 EDP Connector (EDP1)

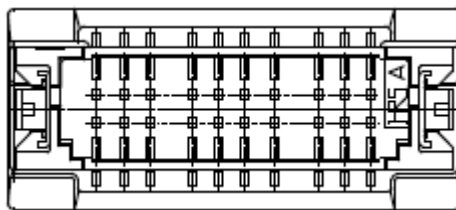


Table 2.46: EDP Connector (EDP1)

Pin	Signal	Pin	Signal
1	GND	2	GND
3	TX0-	4	TX3-
5	TX0+	6	TX3+
7	GND	8	NC
9	TX1-	10	GND
11	TX1+	12	AUX-
13	GND	14	AUX+
15	TX2-	16	GND
17	TX2+	18	EDP_HPDP
19	+VDD_EDP(*)	20	+VDD_EDP(*)

Note! (*) Depends on JEDP1 Jump Setting.



2.2.45 IMVP9.2 Programming Header (VR_PMB1)

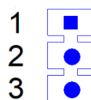


Table 2.47: IMVP9.2 Programming Header (VR_PMB1)

Pin	Signal
1	VR_+VCORE_SCLK
2	GND
3	VR_+VCORE_SDATA

2.2.46 DDR5 U-DIMM Socket (DIMMA1/DIMMA2/DIMMB1/DIMMB2)

Please see JEDEC STANDARD.

Chapter 3

BIOS Operation

3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning special features on or off. This chapter describes the basic navigation of the AIMB-589 setup screens.

3.2 BIOS Setup

The AIMB-589 Series system has AMI BIOS built in, with a CMOS SETUP utility that allows users to configure required settings or to activate certain system features. The CMOS SETUP saves the configuration in the CMOS RAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the CMOS RAM.

When the power is turned on, press the button during the BIOS POST (Power-On Self-Test) to access the CMOS SETUP screen.

Table 3.1: Control Keys

< ↑ >< ↓ >< ← >< → >	Move to select item
<Enter>	Select item
<Esc>	Main Menu - Quit and not save changes into CMOS Sub-Menu - Exit current page and return to Main Menu
<Page Up/+>	Increase the numeric value or make changes
<Page Down/->	Decrease the numeric value or make changes
<F1>	General help, for Setup Sub Menu
<F2>	Item Help
<F3>	Loads previous values
<F4>	Load Setup Defaults
<F10>	Save all CMOS changes

3.2.1 Main Menu

Press to enter the AMI BIOS CMOS Setup Utility. The Main Menu will appear on the screen. Use the arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the legend.

Above the legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

■ System Time/System Date

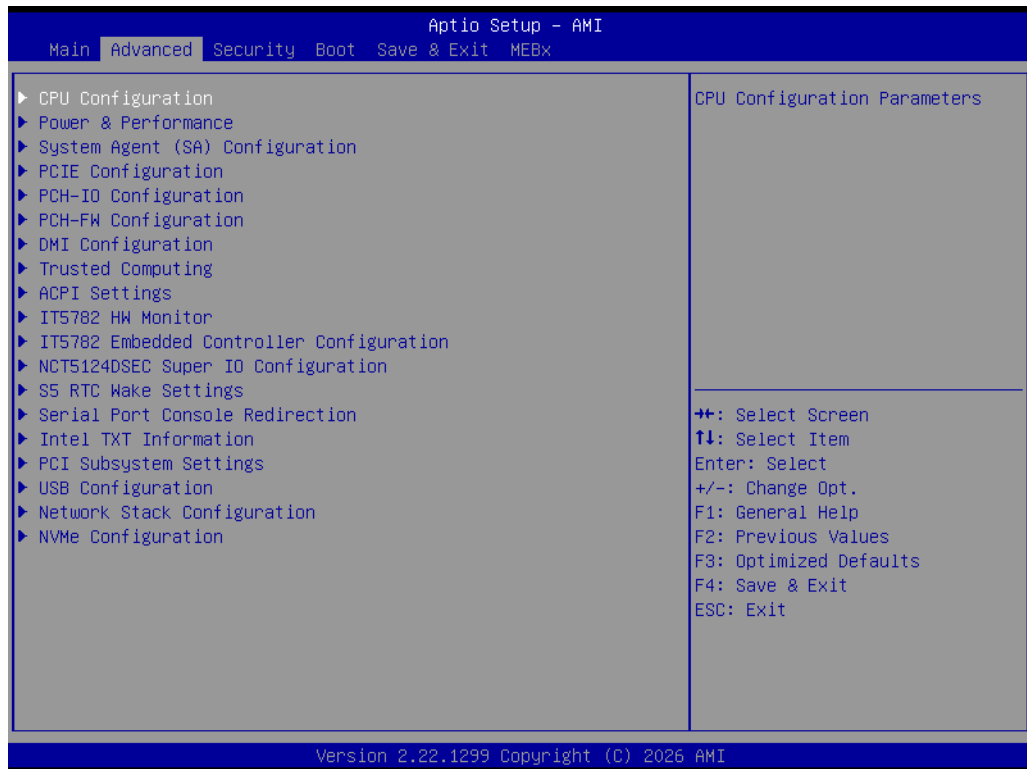
Use this option to change the system time and date. Highlight the System Time or System Date using the keys. Enter new values via the keyboard. Press the arrow keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-589 setup menu to enter the Advanced BIOS setup page. Users can select any item in the left frame of the screen, such as CPU configuration. Select an Advanced BIOS setup option by highlighting the text using the keys. All Advanced BIOS setup options are described in this section. The Advanced BIOS setup menu screen is shown below. The sub-menus are described in the following pages.

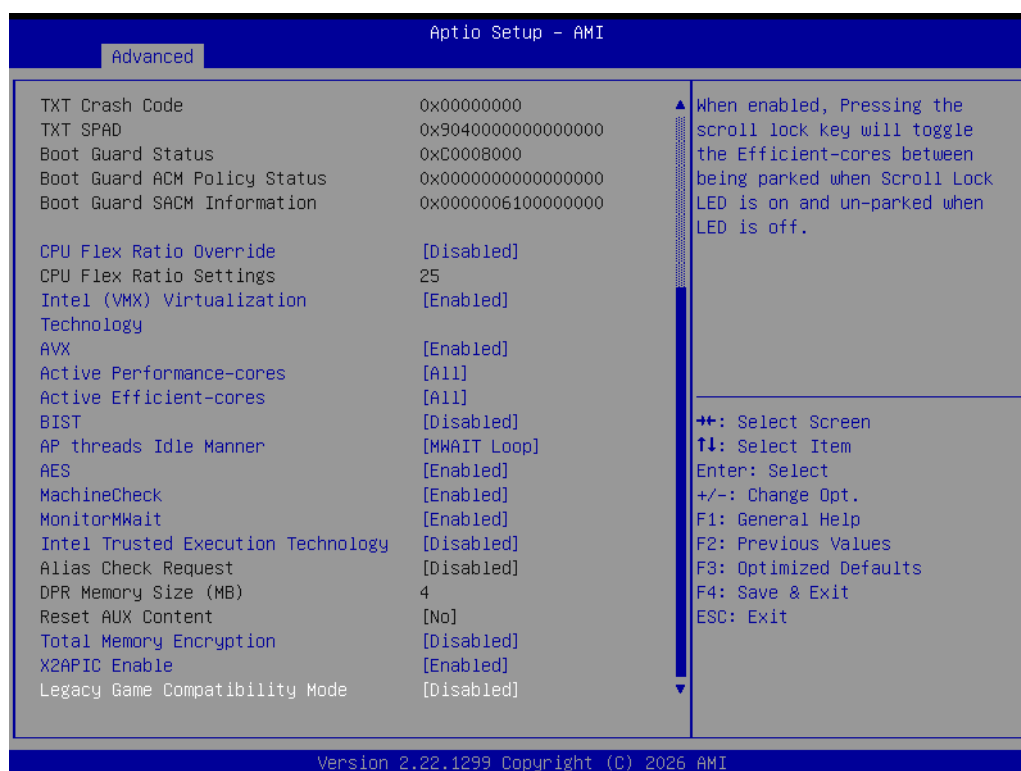
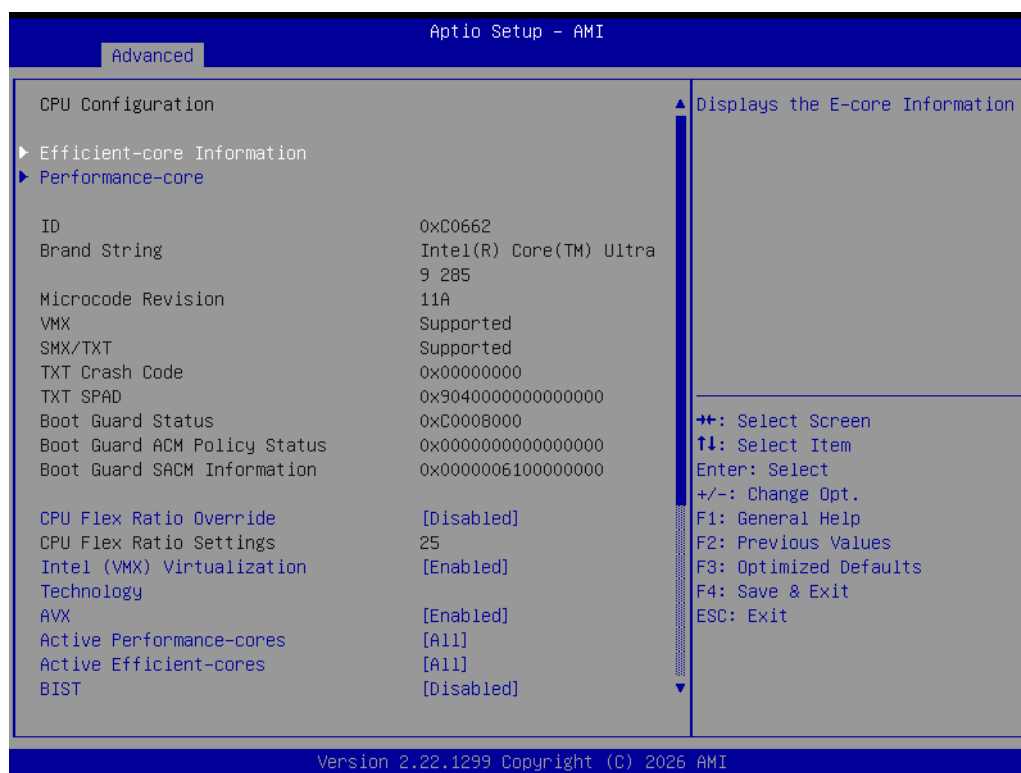
3.2.2.1 CPU Configuration

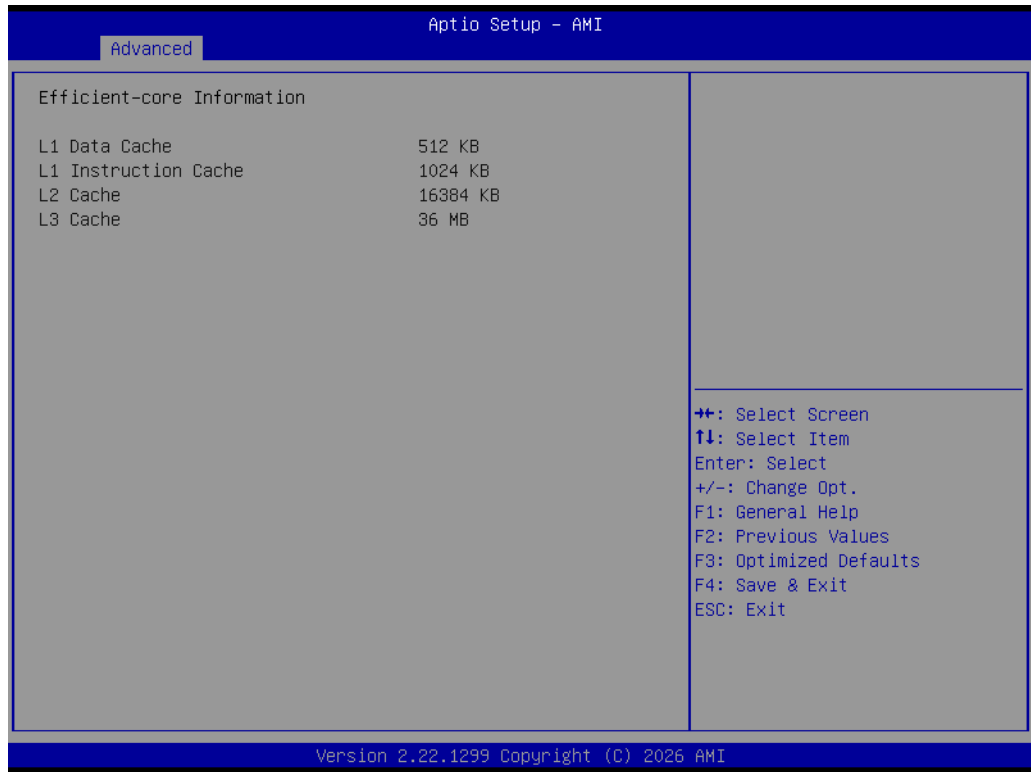
Advanced → CPU Configuration



Efficient-core Information

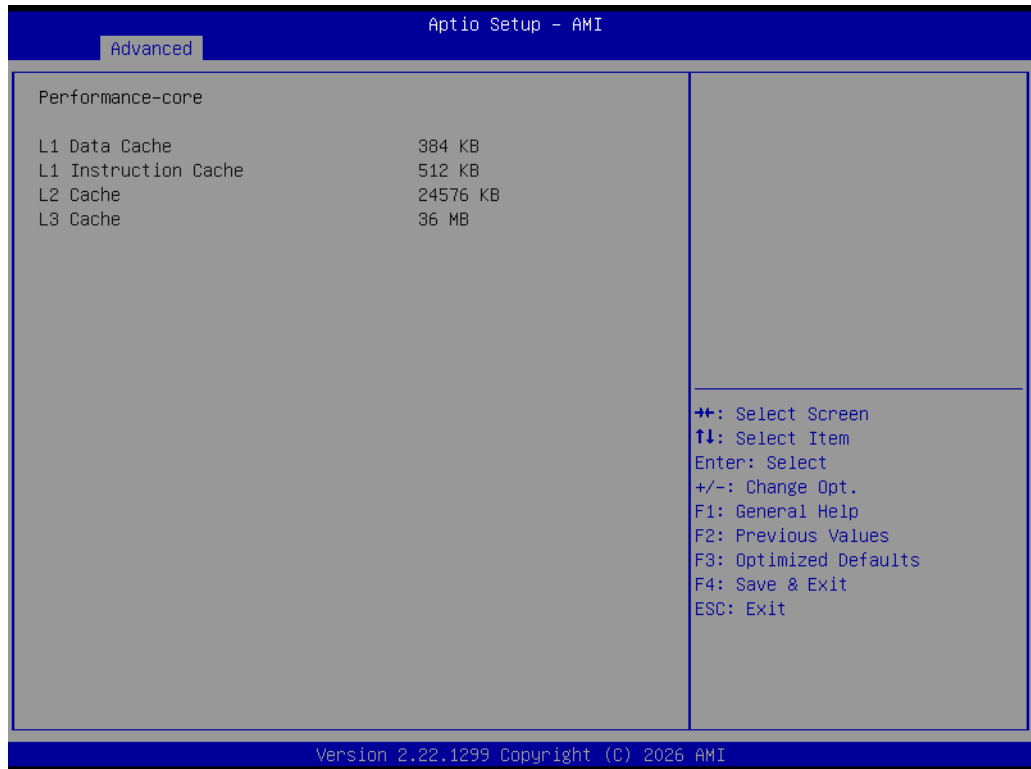
Advanced → CPU Configuration → Efficient-core Information





Performance-core Information

Advanced → CPU Configuration → Performance-core Information



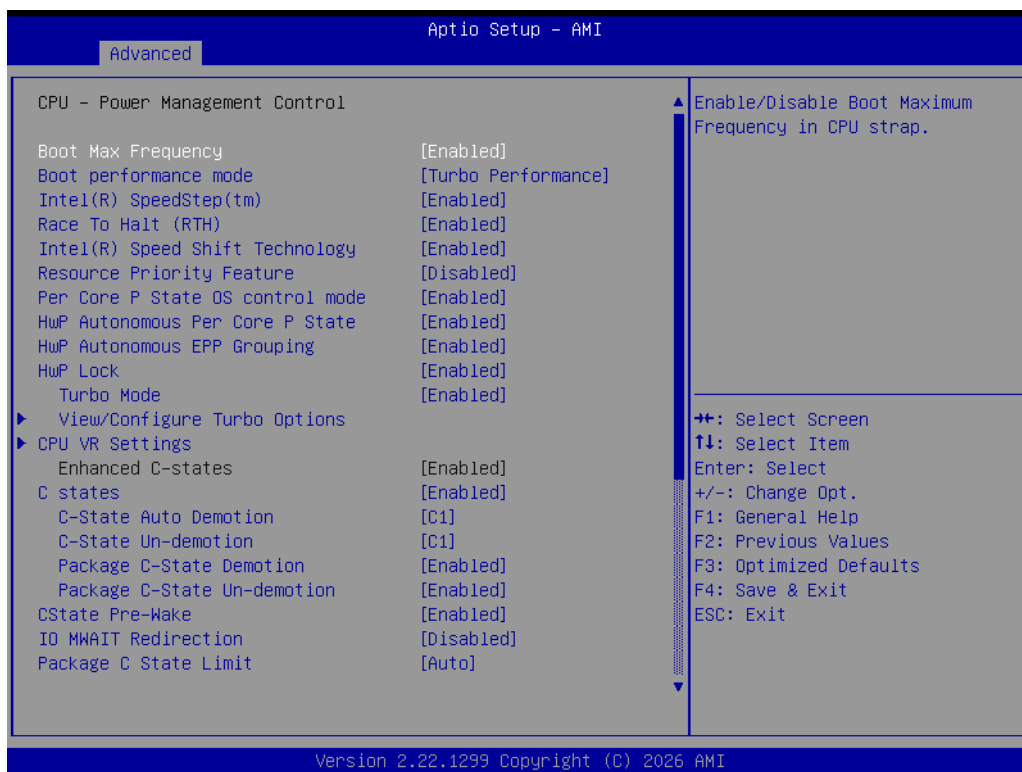
3.2.2.2 Power & Performance

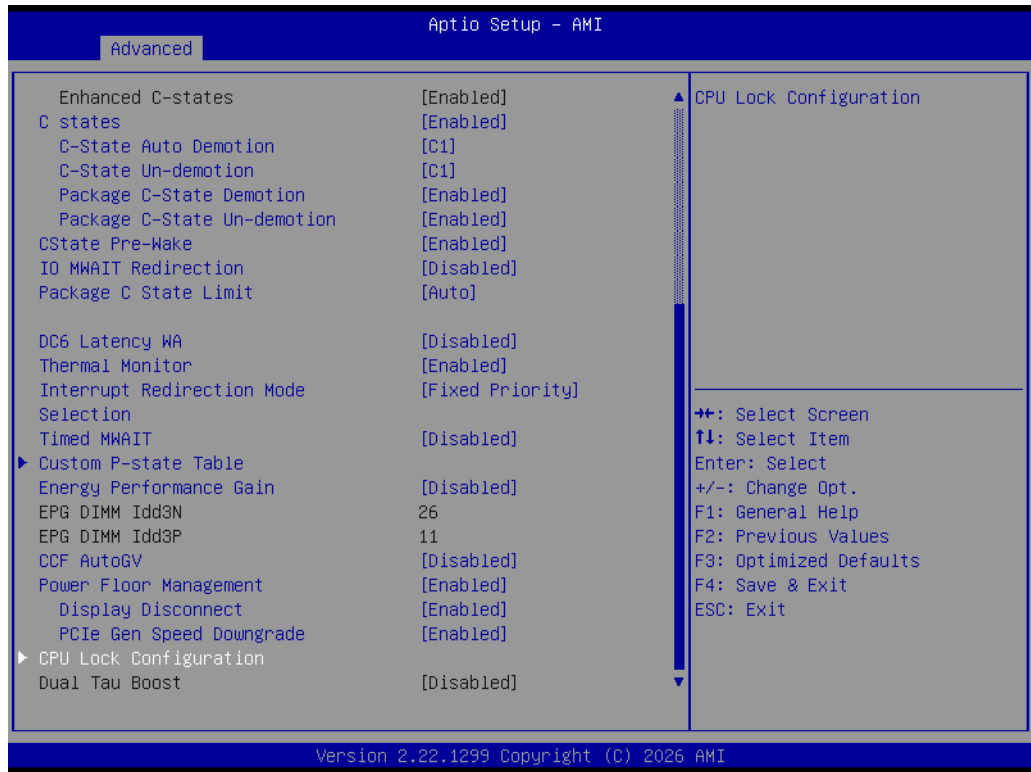
Advanced → Power & Performance



CPU – Power Management Control

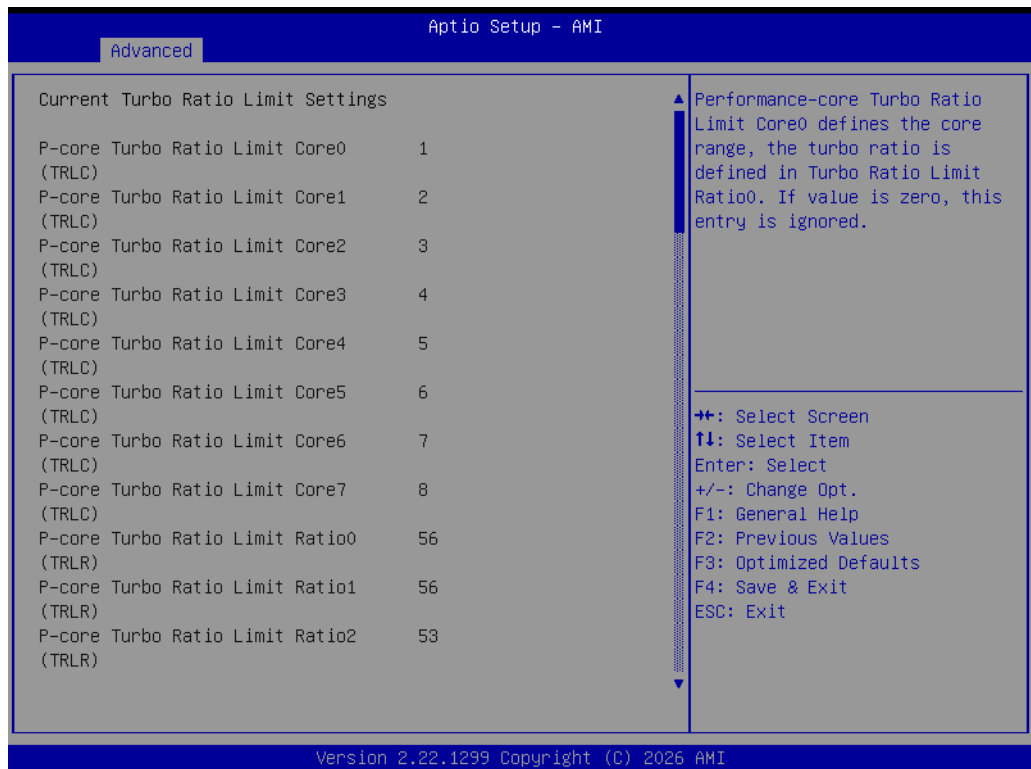
Advanced → Power & Performance → CPU – Power Management Control

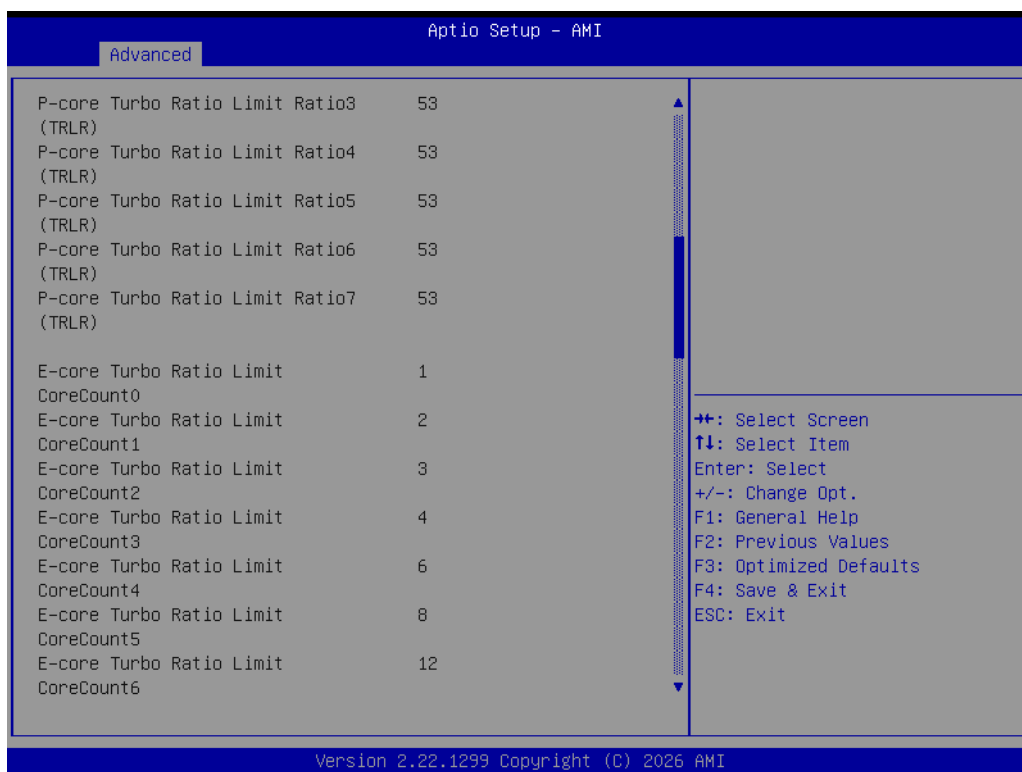




Current Turbo Settings

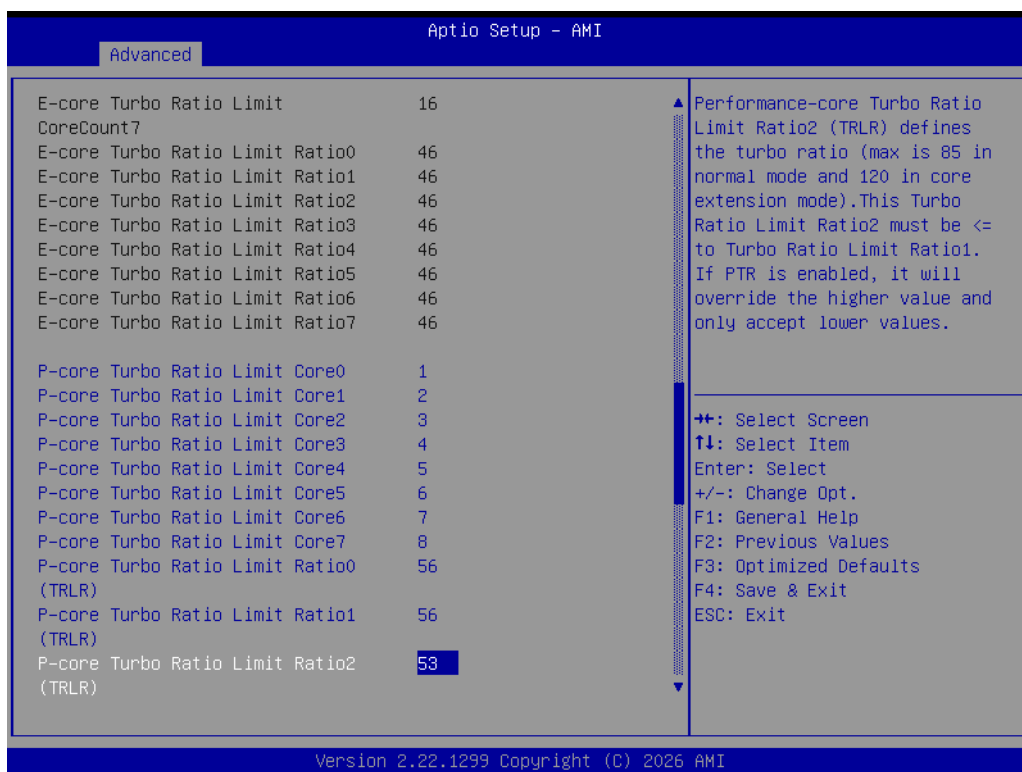
Advanced → Power & Performance → CPU – Power Management Control → View/Configure Turbo Ratio

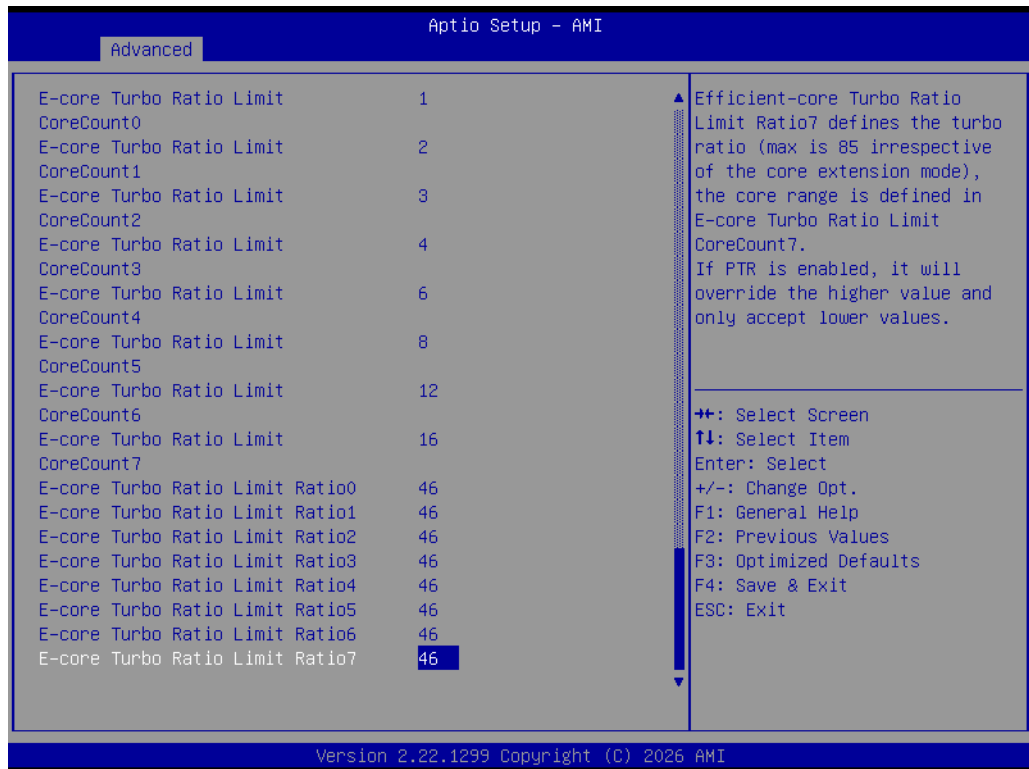
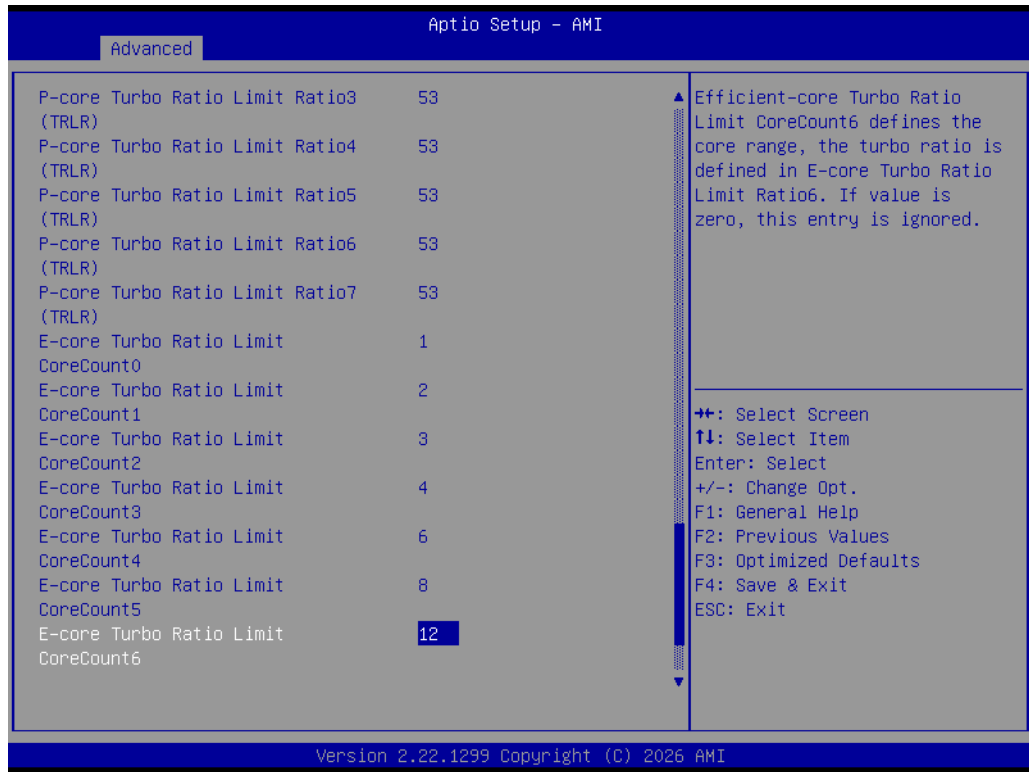




Turbo Ratio Limit Options

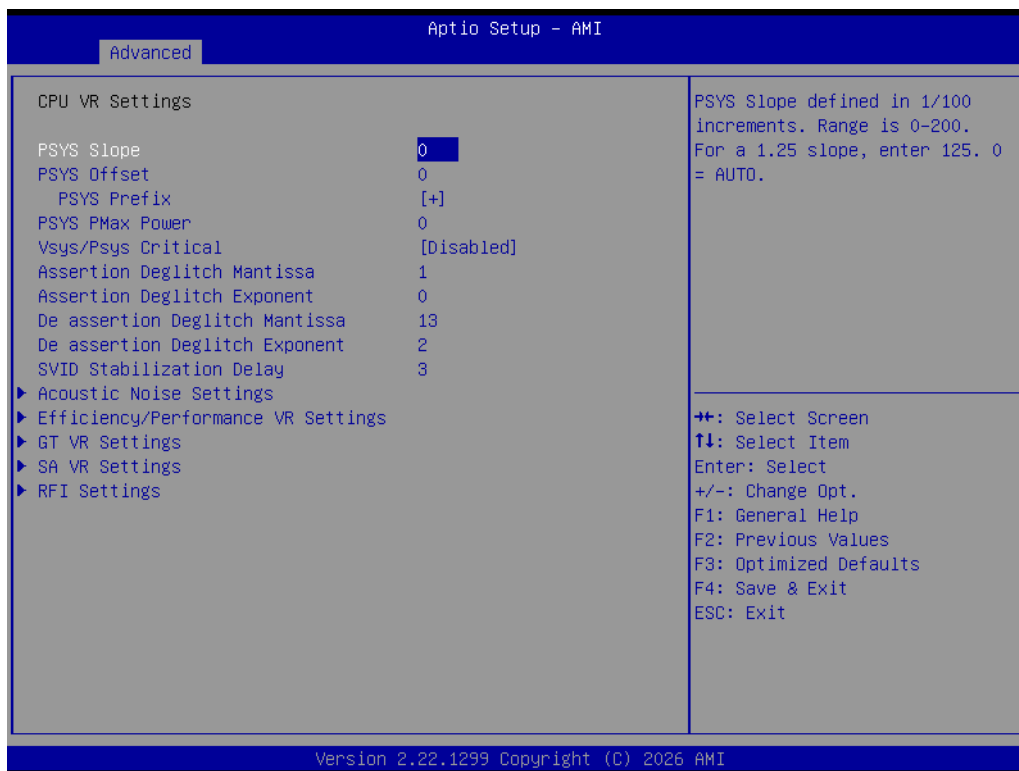
Advanced → Power & Performance → CPU – Power Management Control → View/Configure Turbo Ratio → Turbo Ratio Limit Options





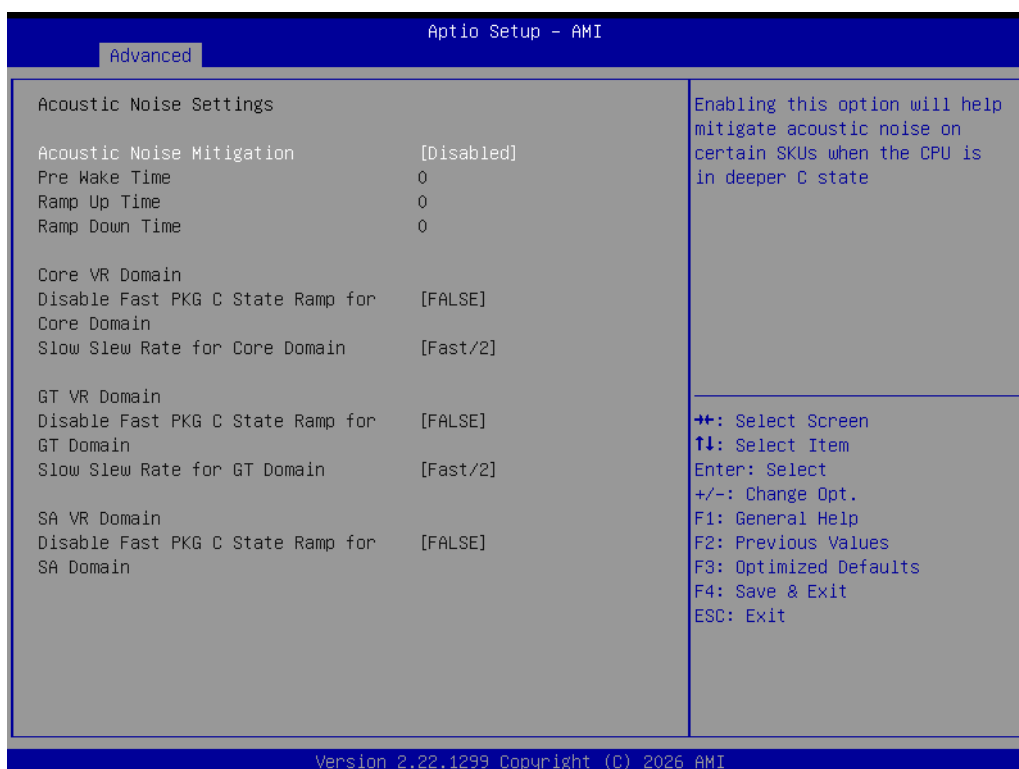
CPU VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings



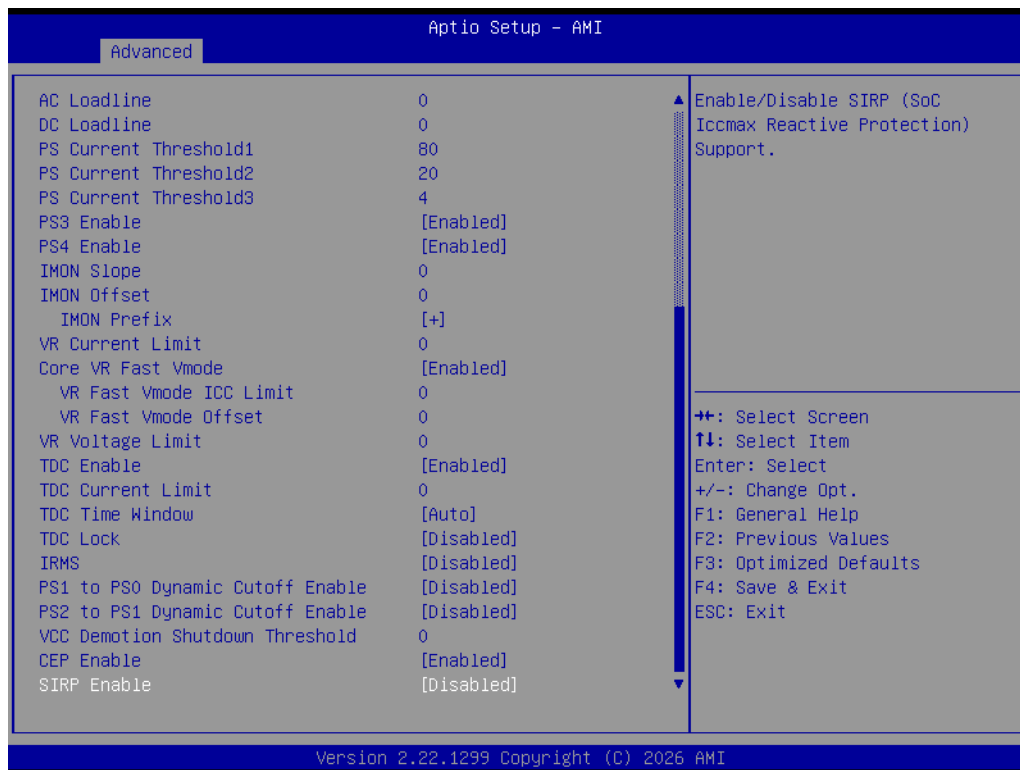
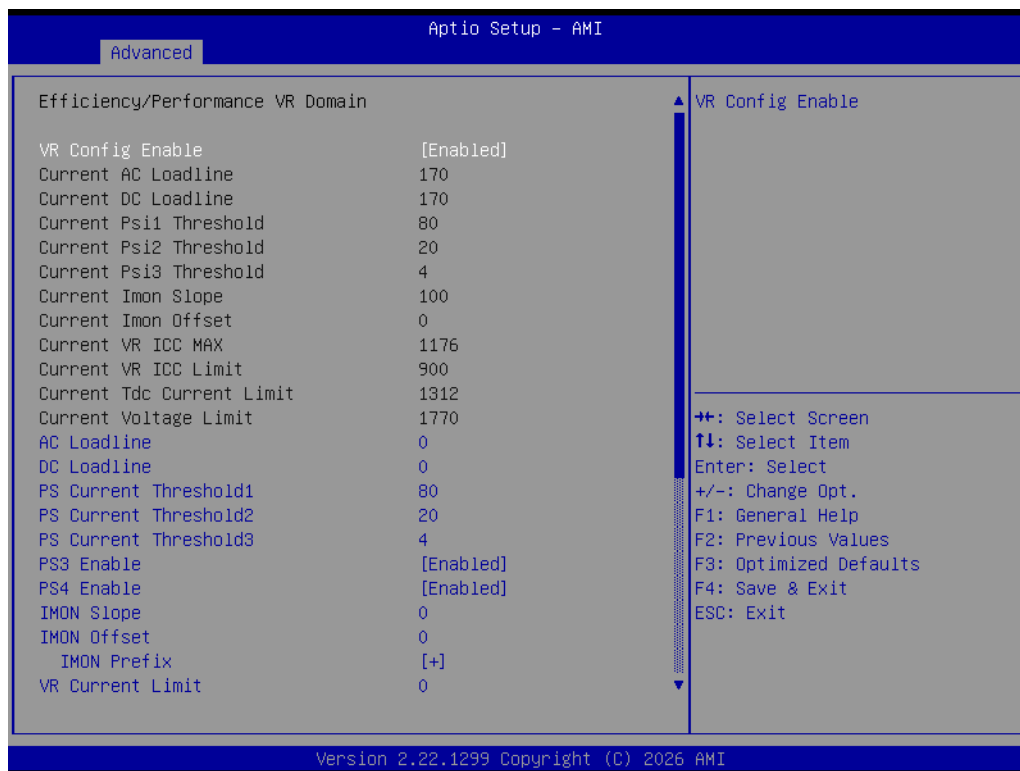
Acoustic Noise Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Acoustic Noise Settings



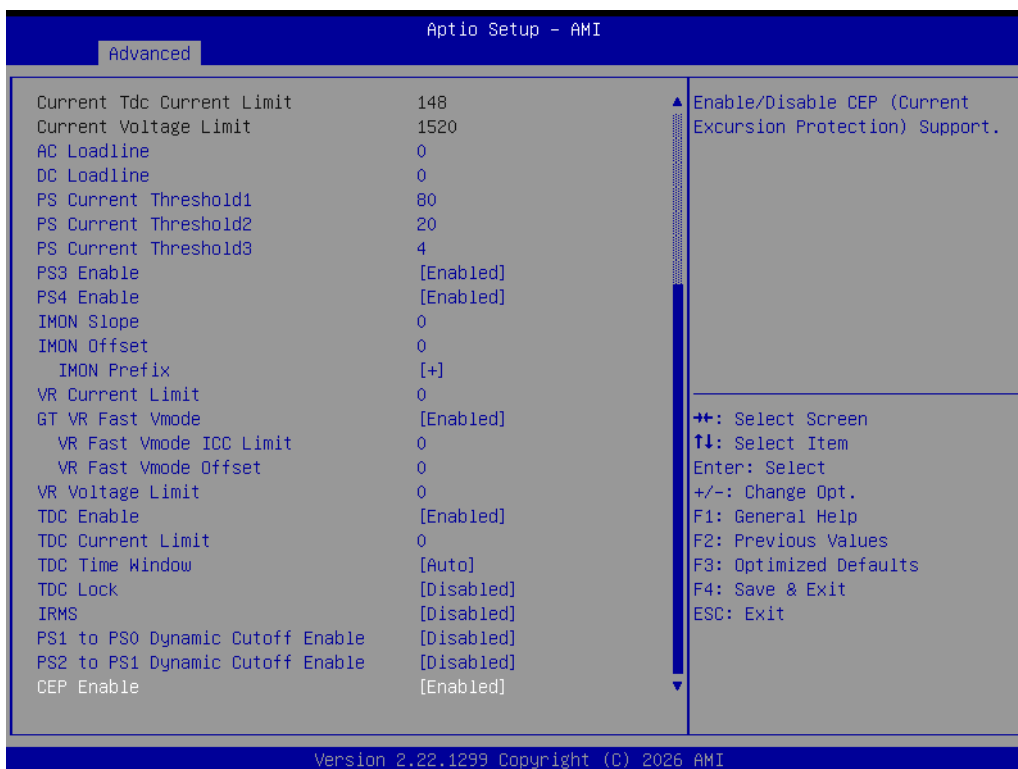
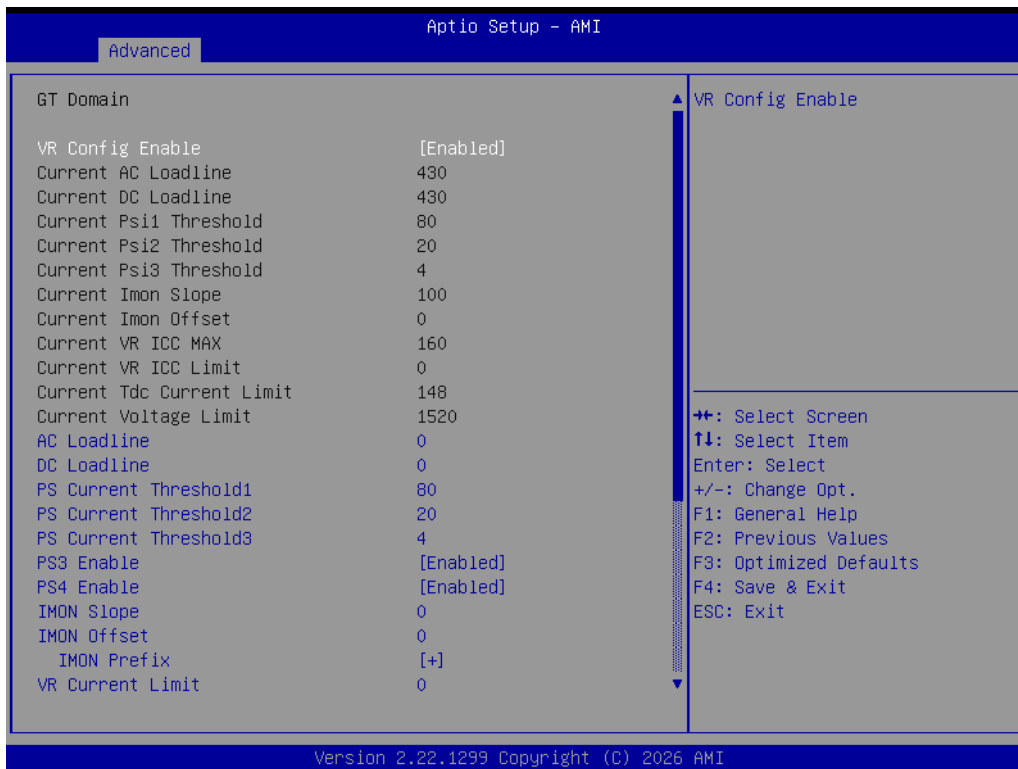
Efficiency/Performance VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → Efficiency/Performance VR Settings



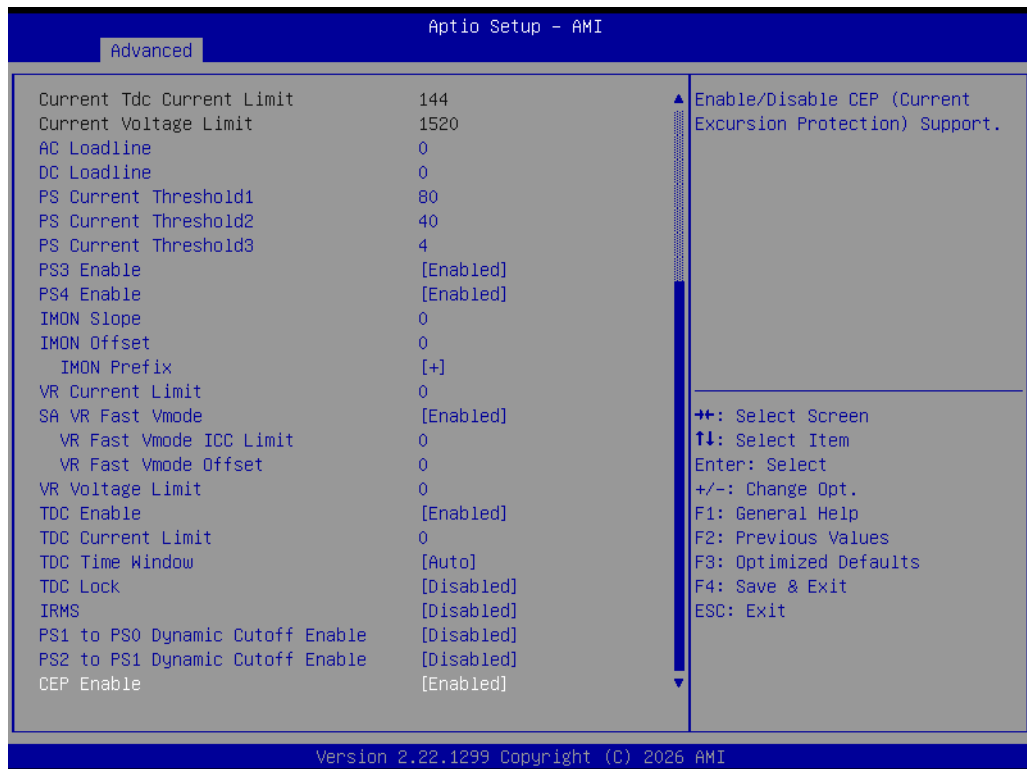
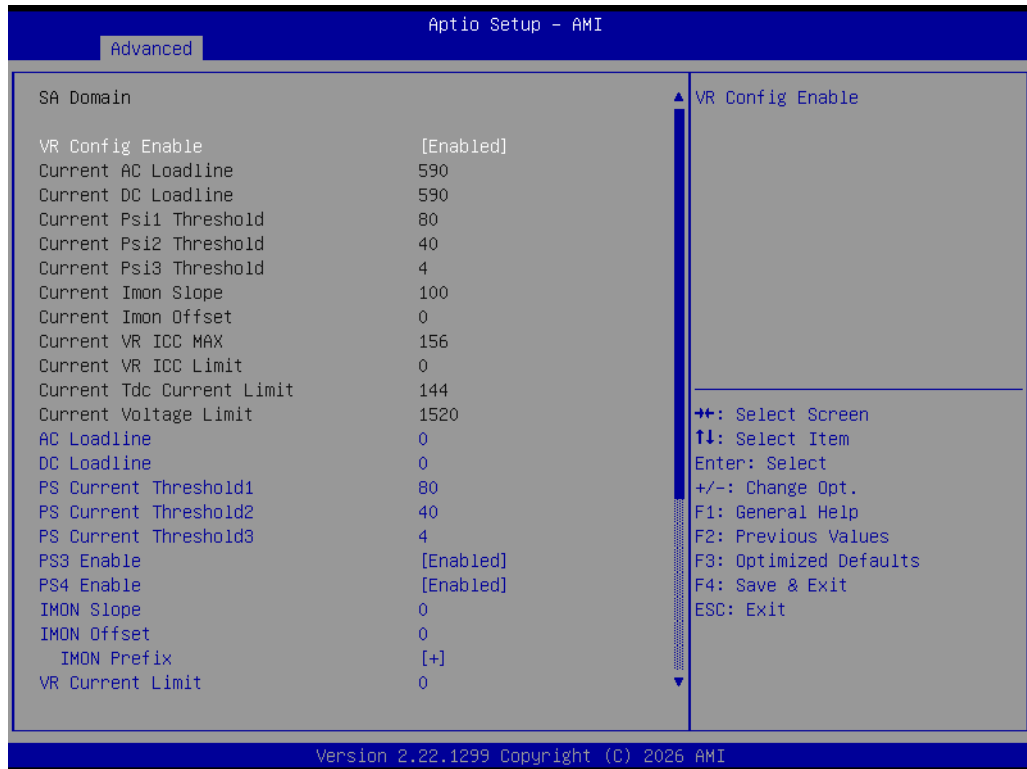
GT VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → GT VR Settings



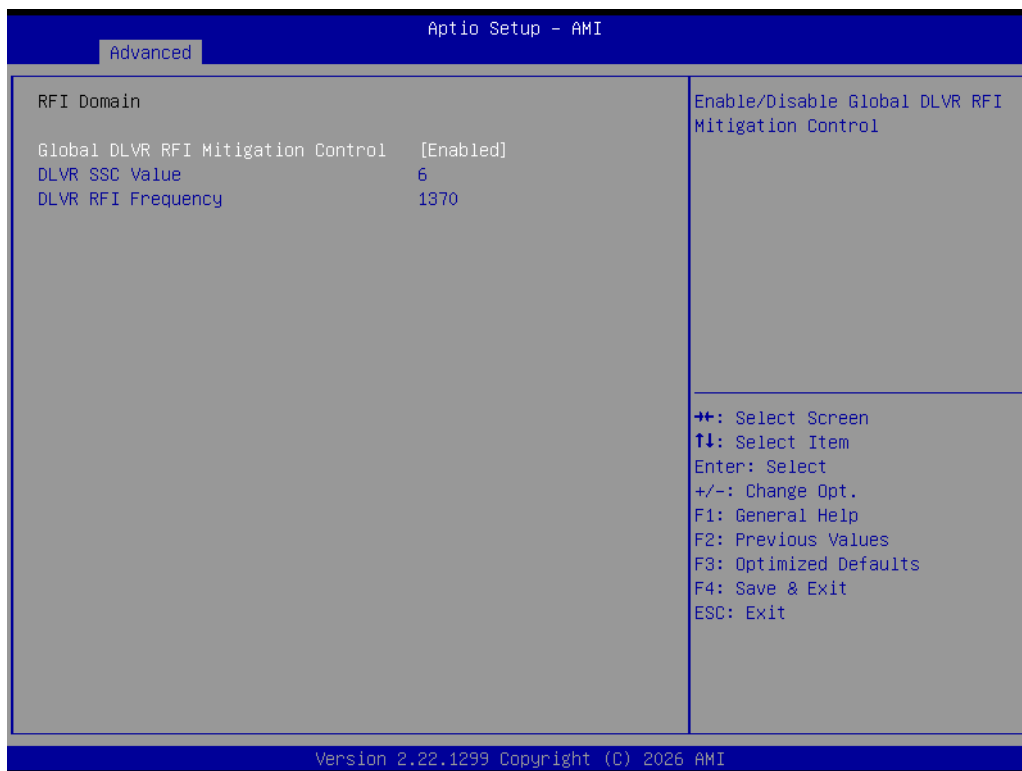
SA VR Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → SA VR Settings



RFI Settings

Advanced → Power & Performance → CPU – Power Management Control → CPU VR Settings → RFI Settings



Custom P-state Table

Advanced → Power & Performance → CPU – Power Management Control → Custom P-state Table



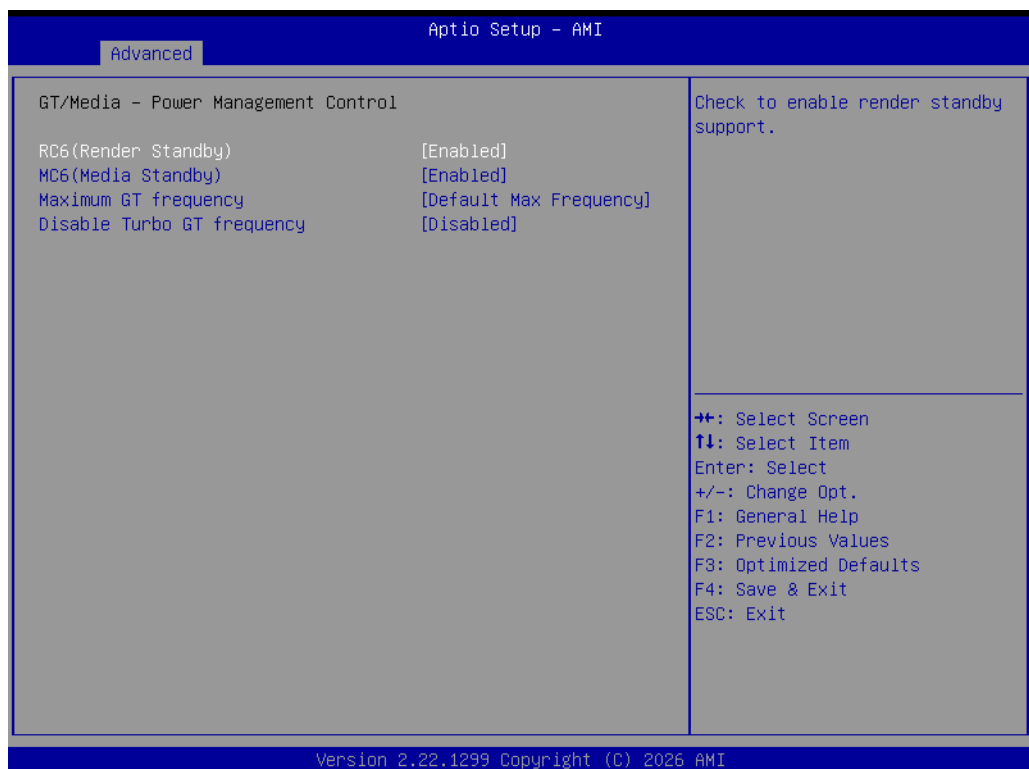
CFG Lock

Advanced → Power & Performance → CPU – Power Management Control → CFG Lock



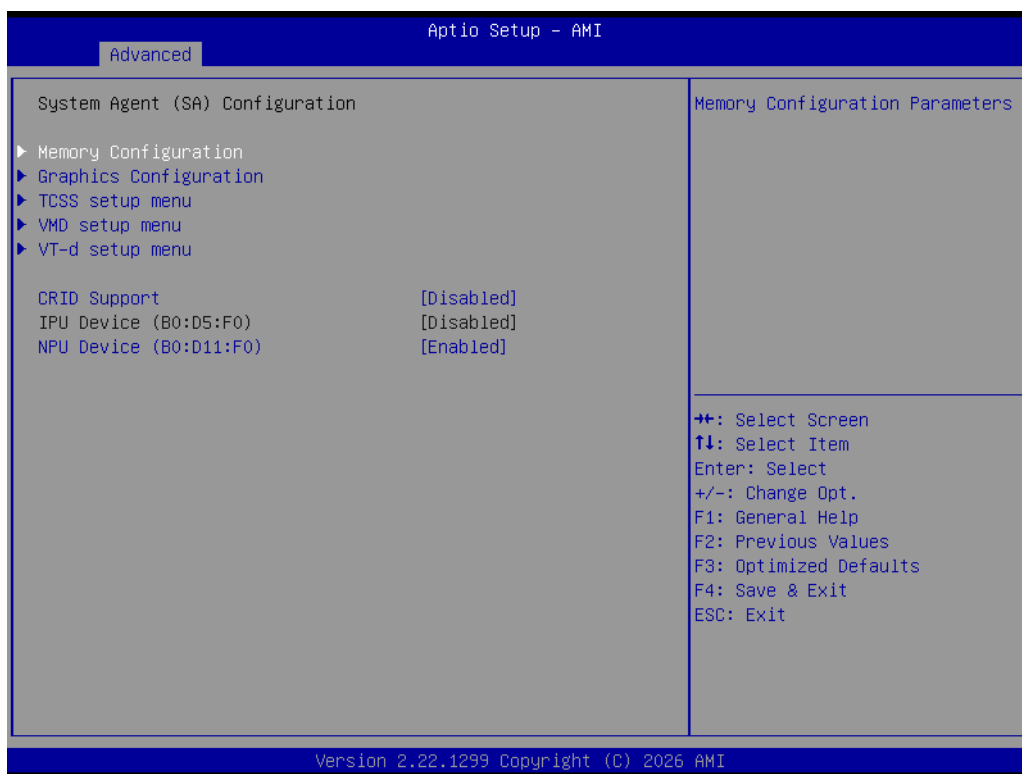
GT/Media – Power Management Control

Advanced → Power & Performance → GT/Media – Power Management Control



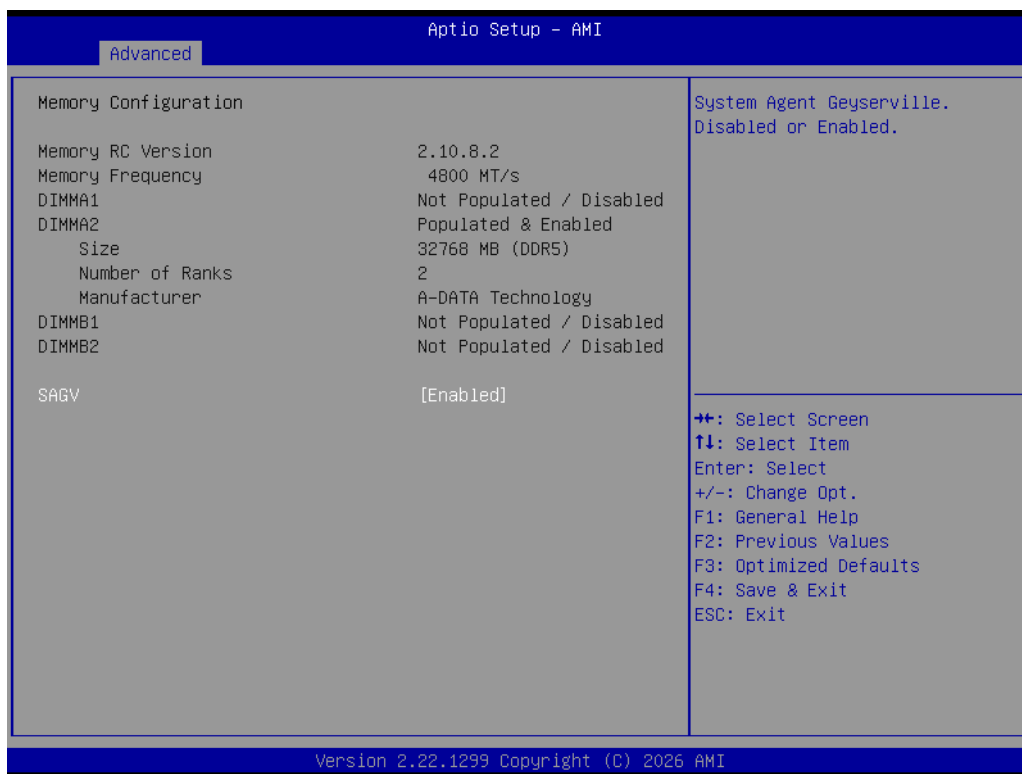
3.2.2.3 System Agent (SA) Configuration

Advanced → System Agent (SA) Configuration



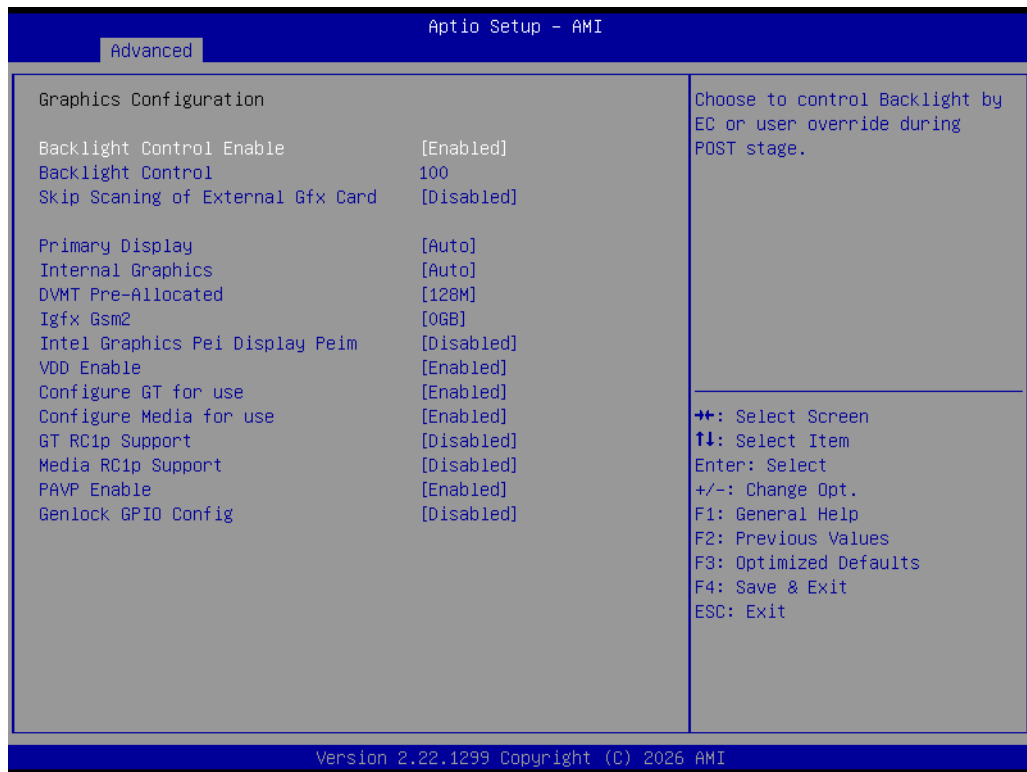
Memory Configuration

Advanced → System Agent (SA) Configuration → Memory Configuration



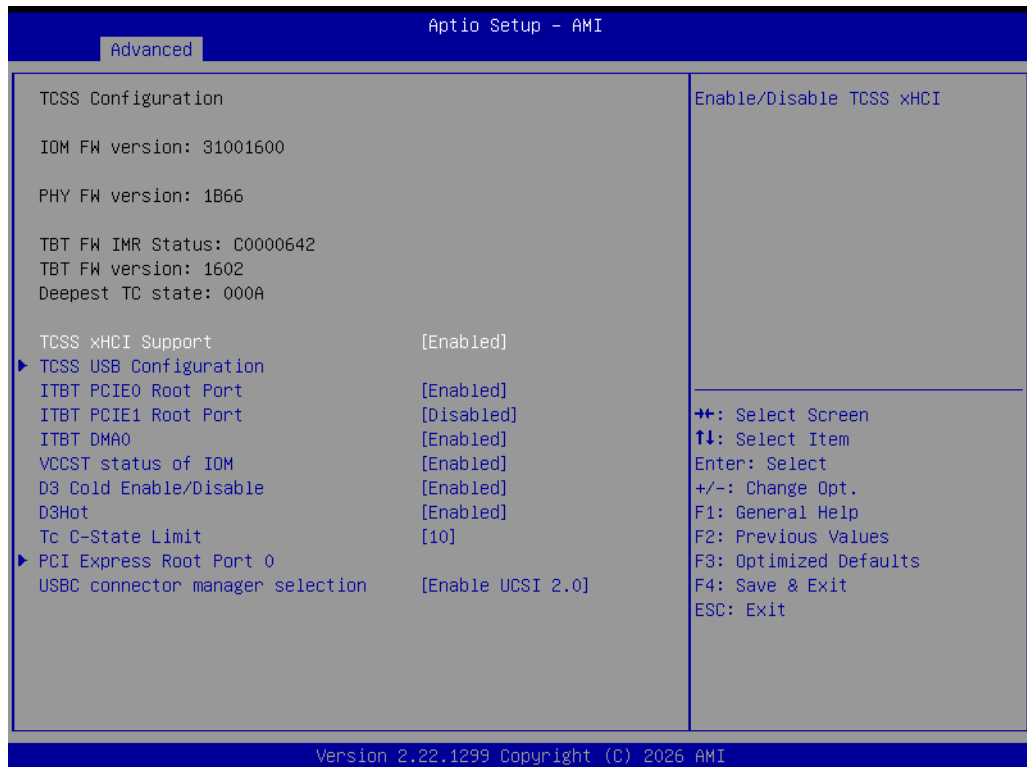
Graphics Configuration

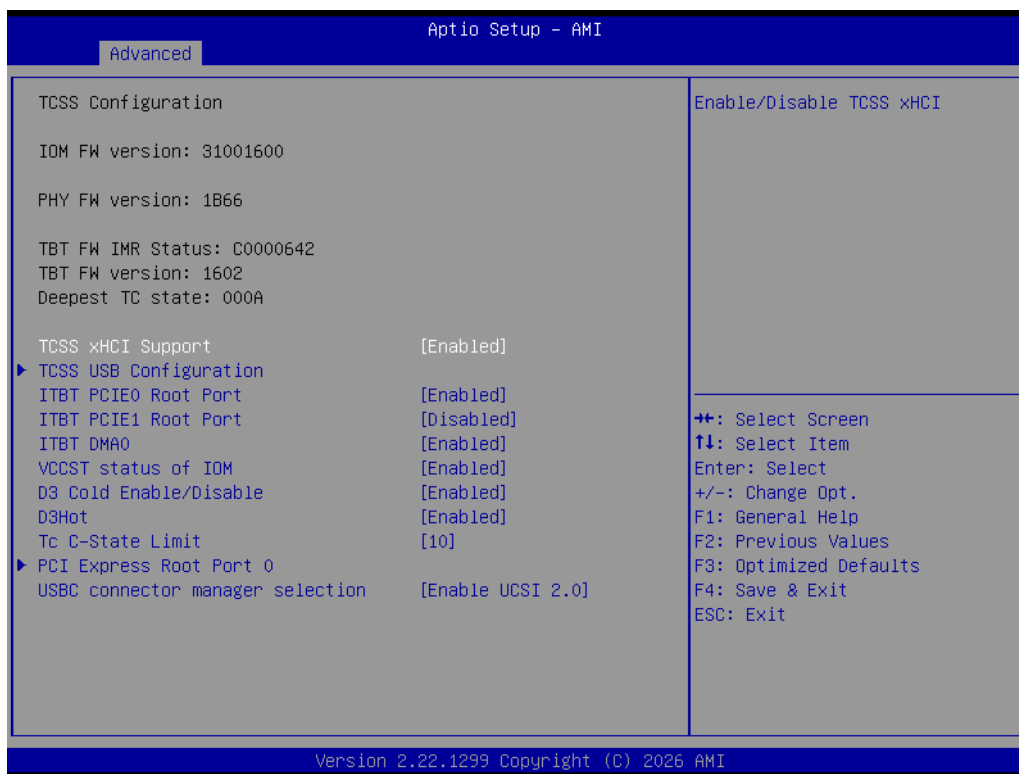
Advanced → System Agent (SA) Configuration → Graphics Configuration

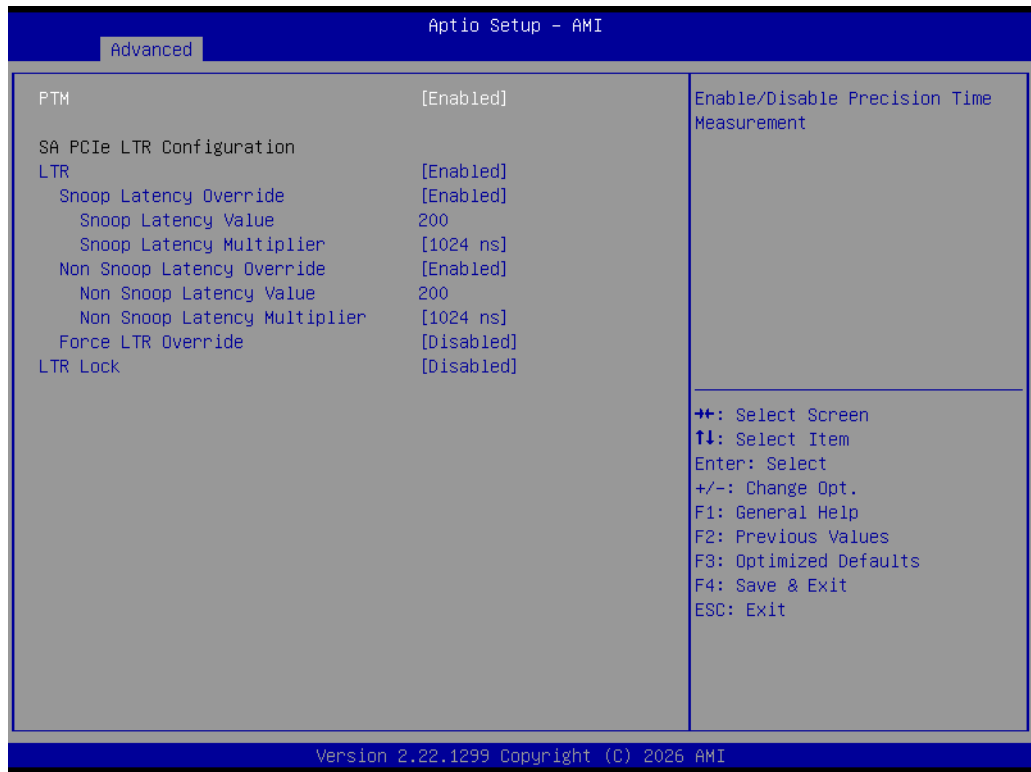


TCSS Configuration

Advanced → System Agent (SA) Configuration → TCSS Configuration

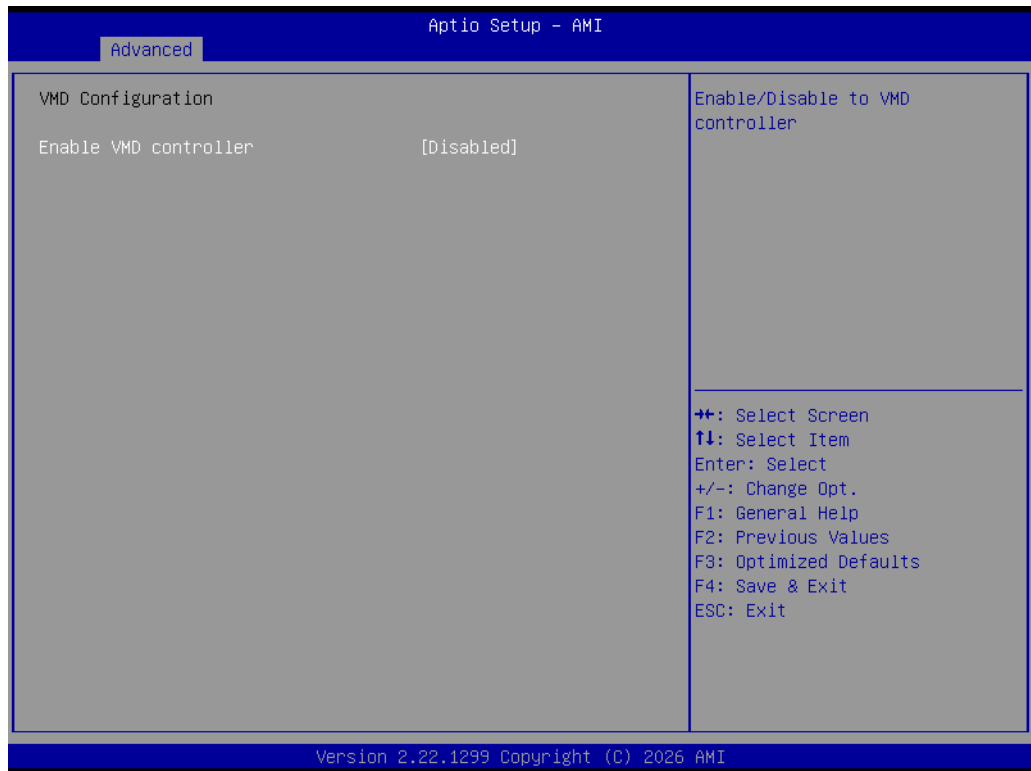






VMD Configuration

Advanced → System Agent (SA) Configuration → VMD Configuration



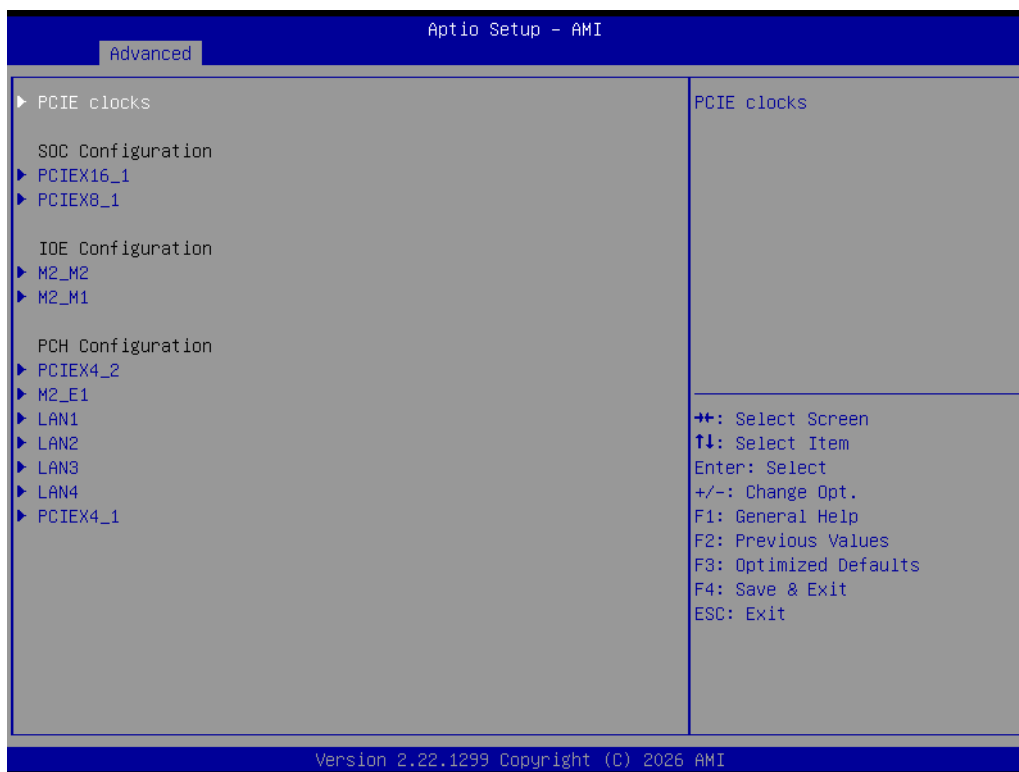
VT-d Configuration

Advanced → System Agent (SA) Configuration → VT-d Configuration



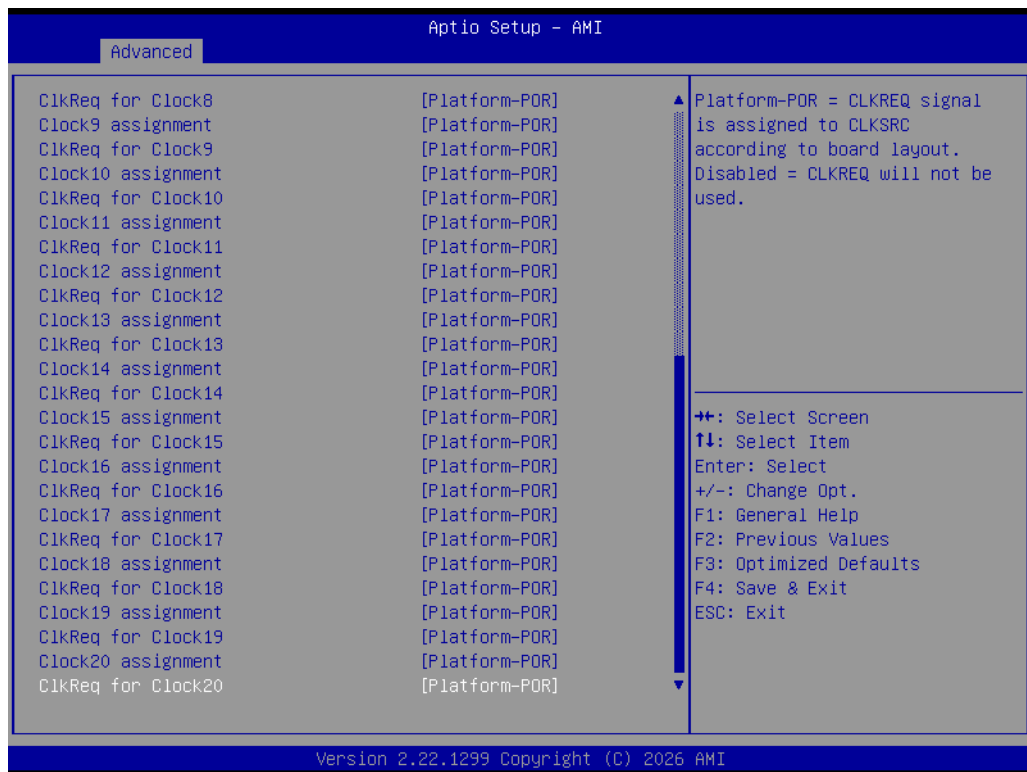
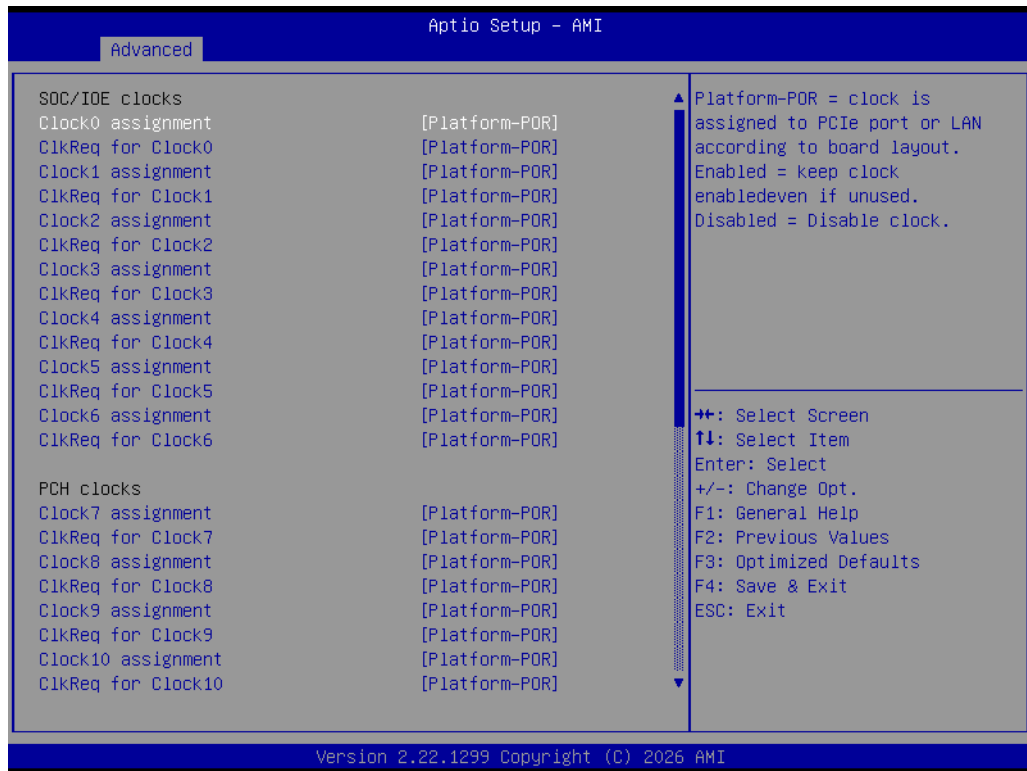
3.2.2.4 PCIE Configuration

Advanced → PCIE Configuration



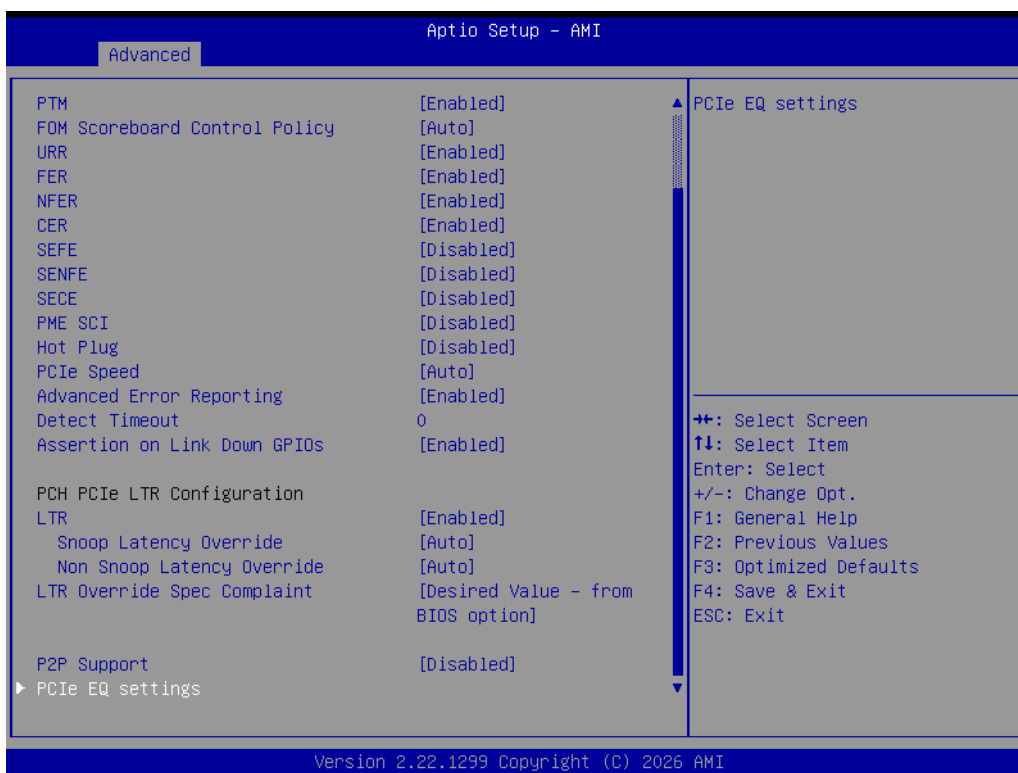
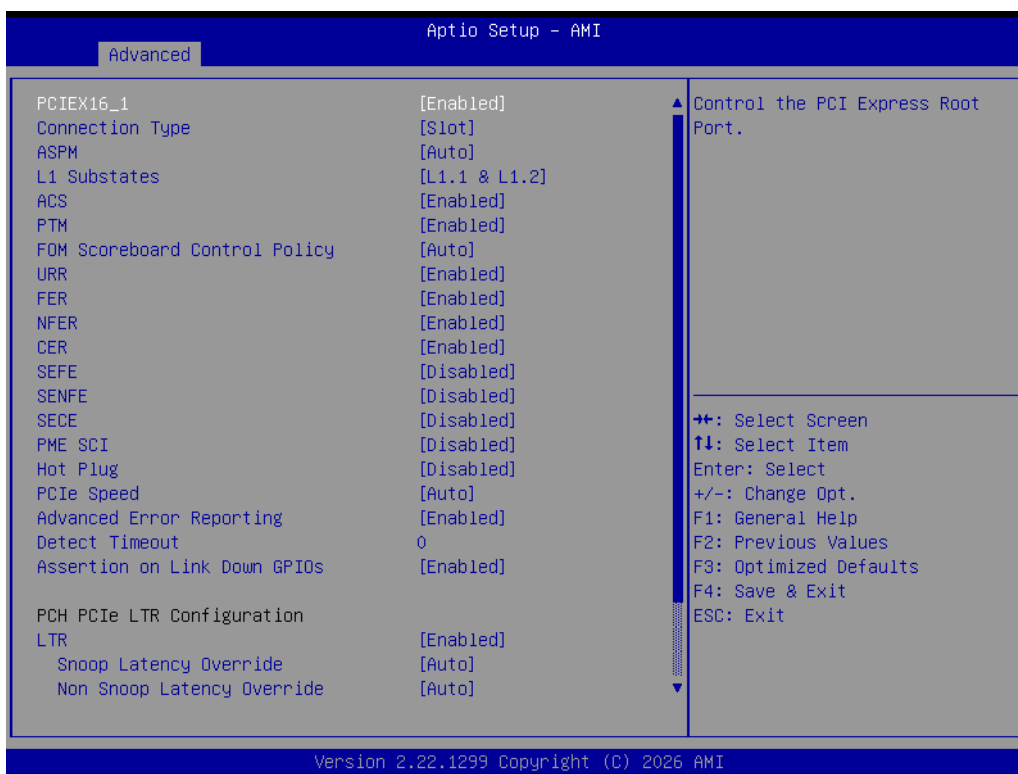
SOC Configuration

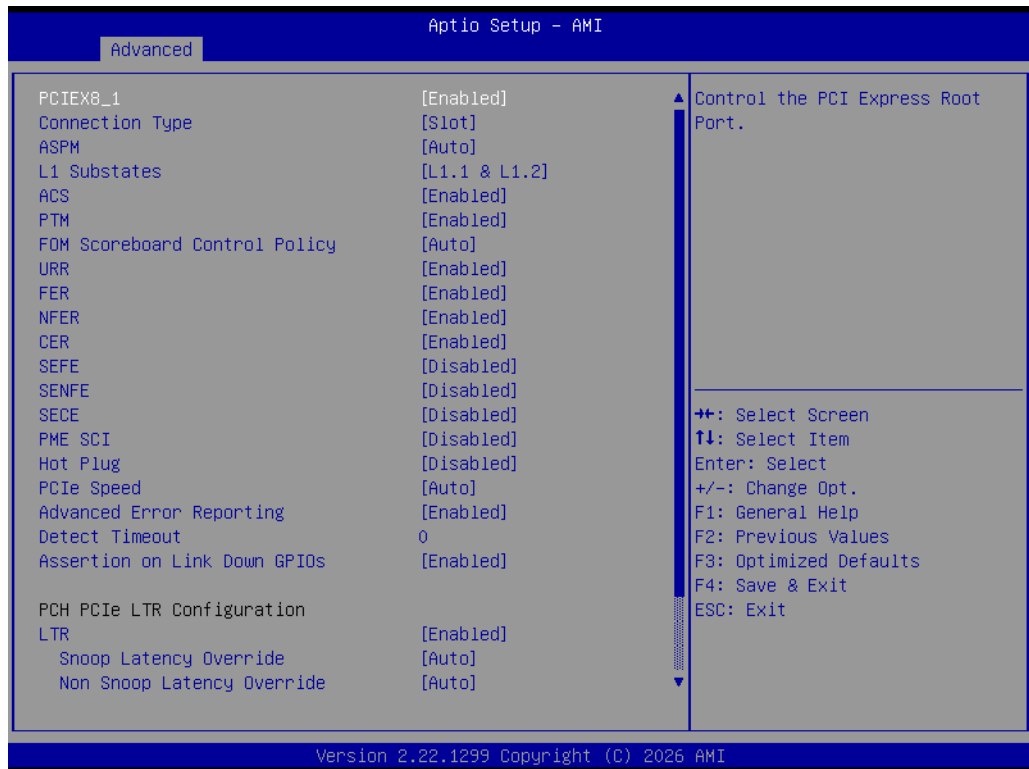
Advanced → PCIE Configuration → SOC Configuration

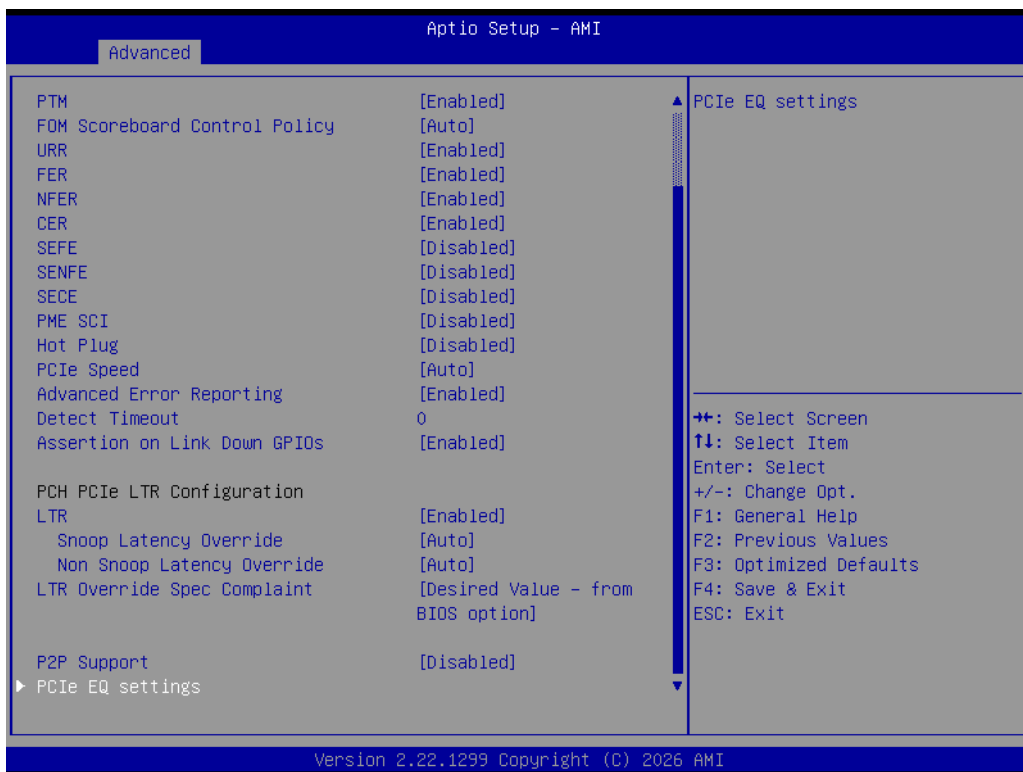


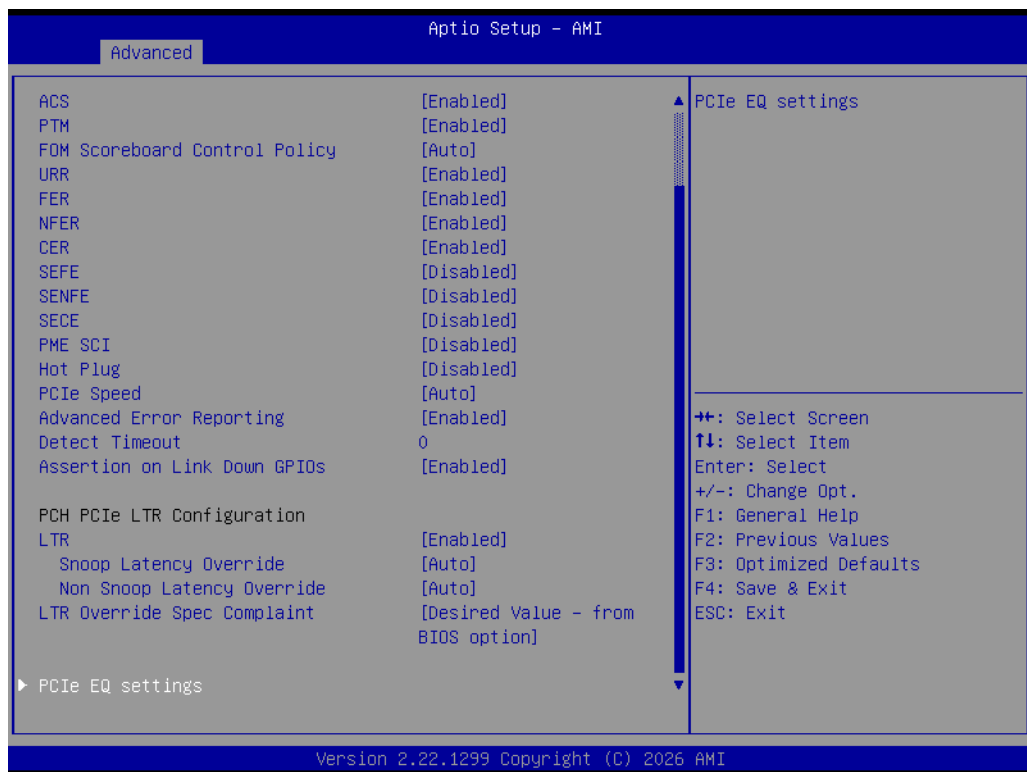
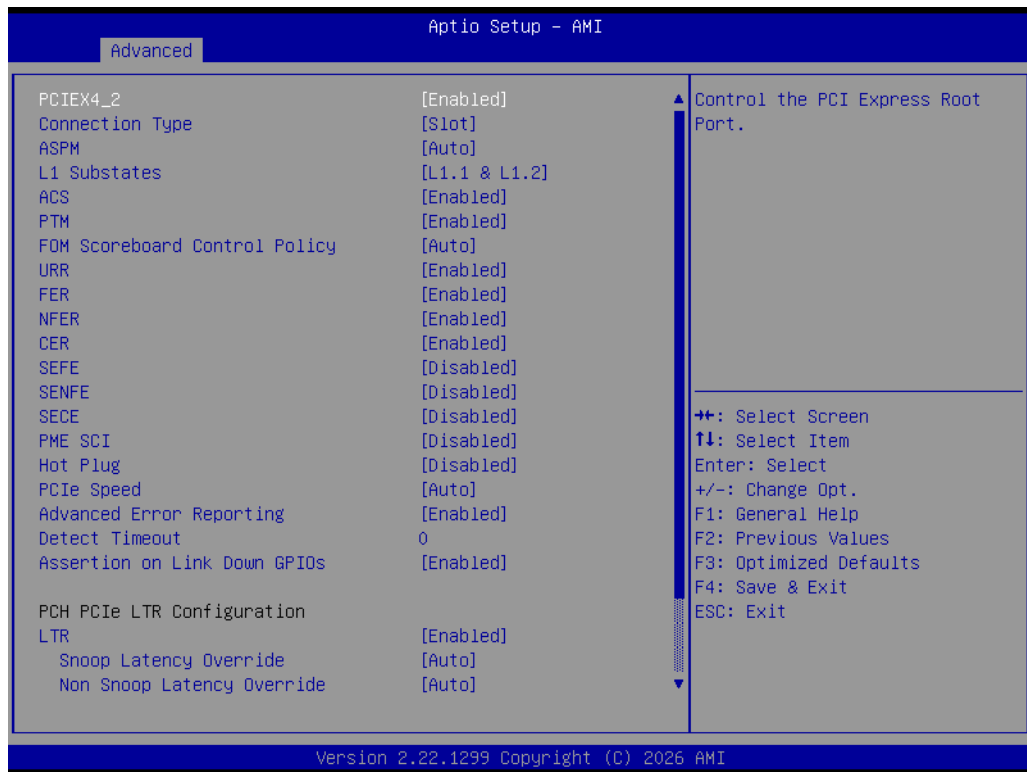
PCIE X16, PCIE X8, PCIE X4

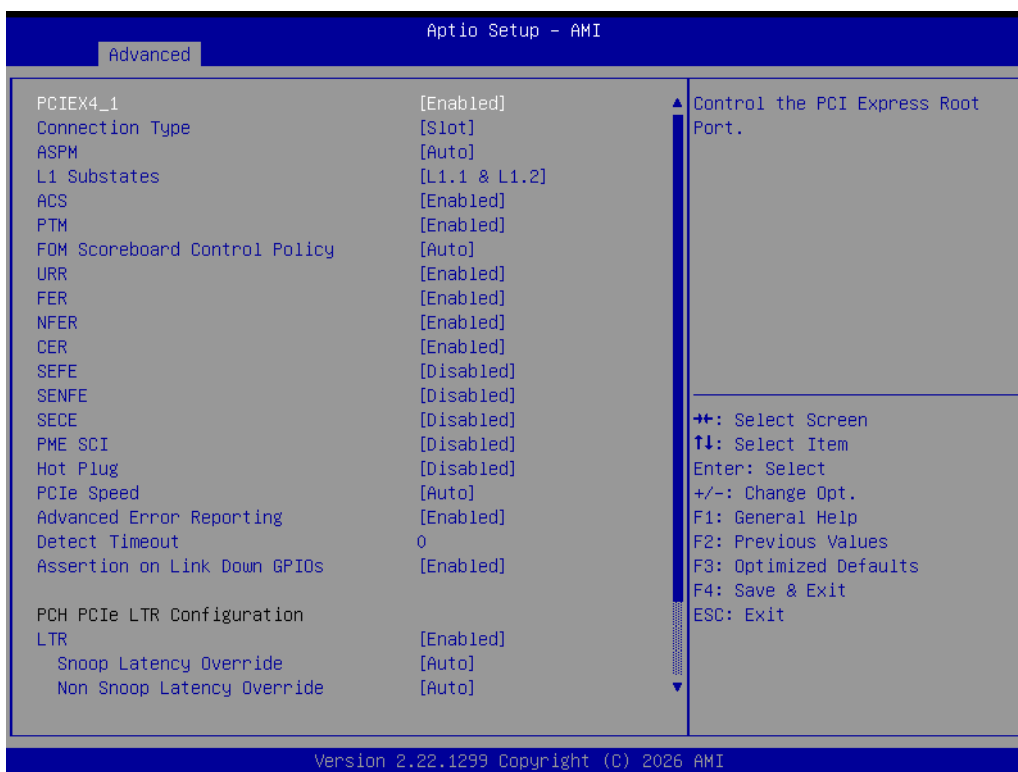
Advanced → PCIE Configuration → PCIE X16, PCIE X8, PCIE X4

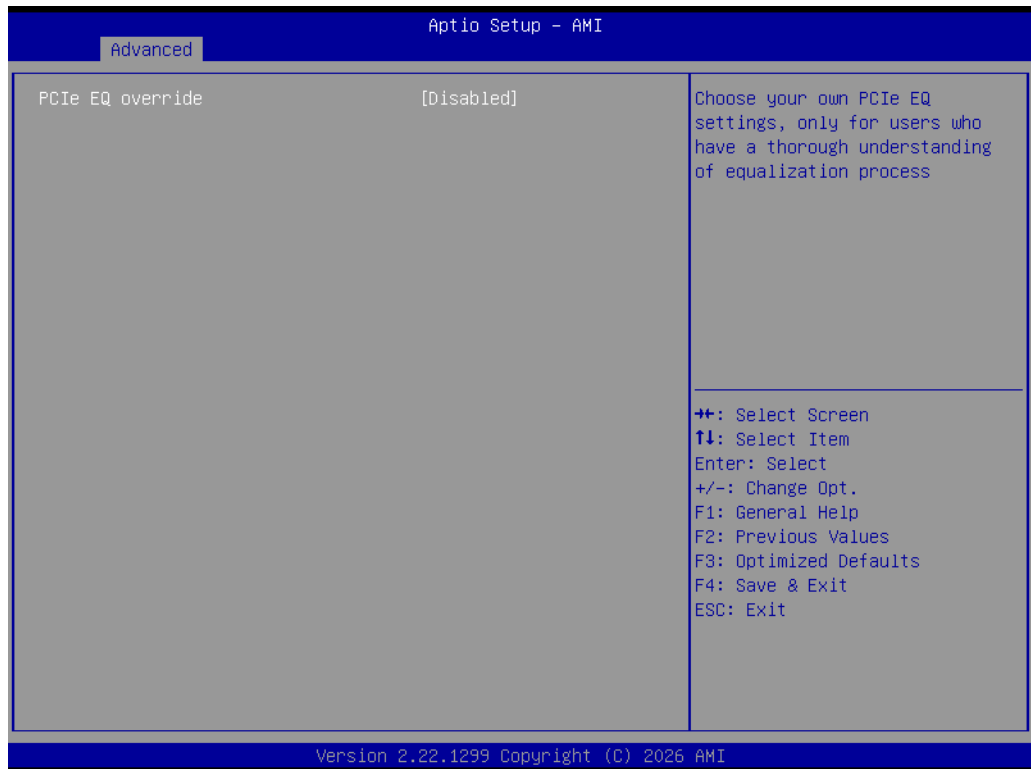
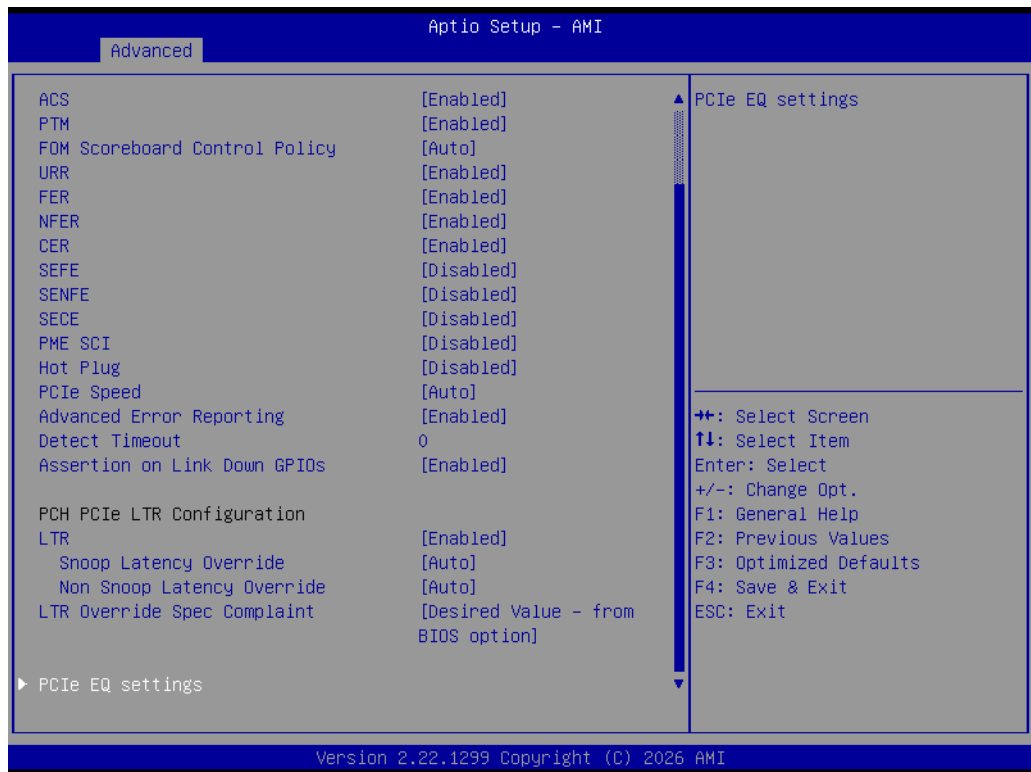










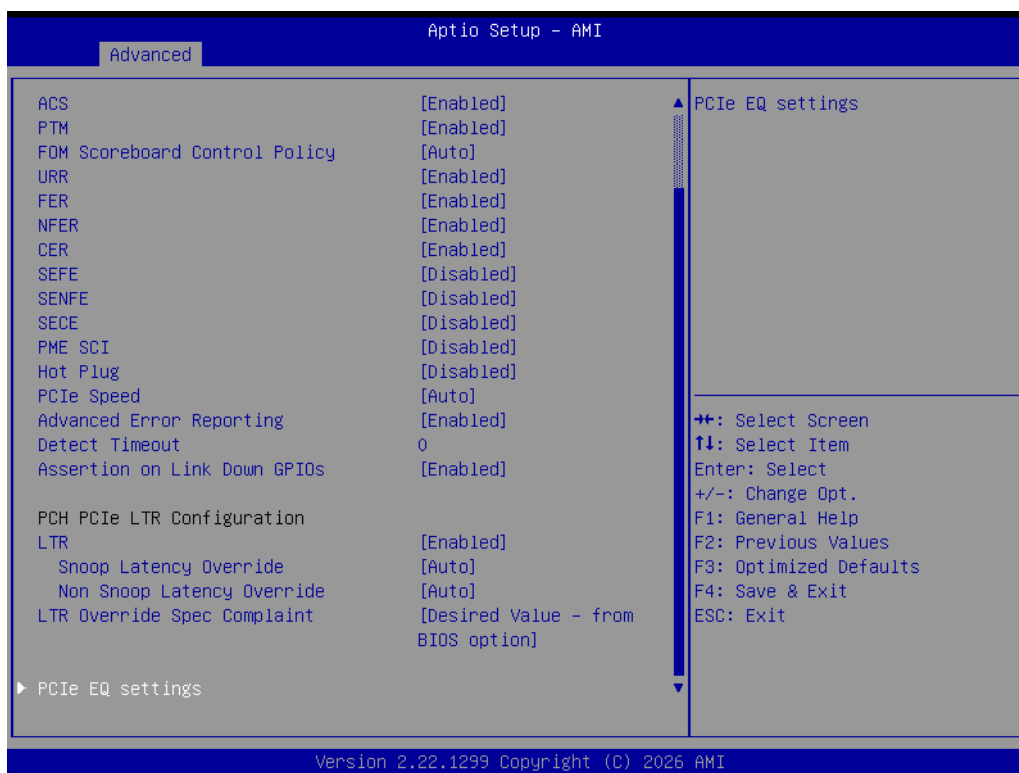
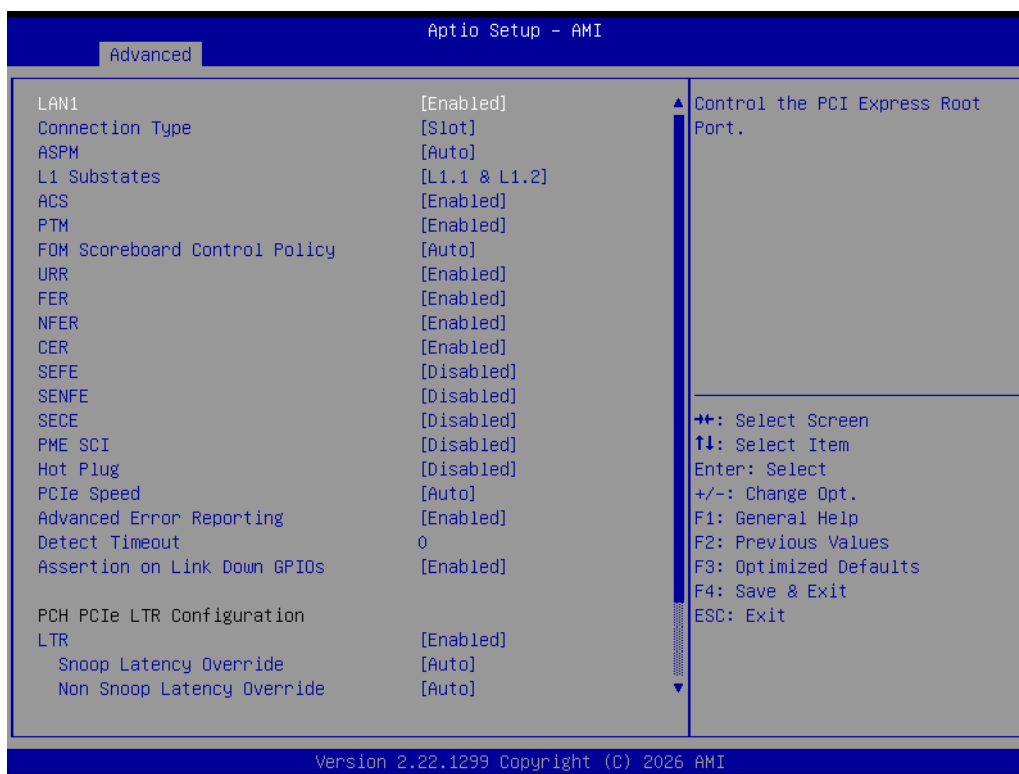


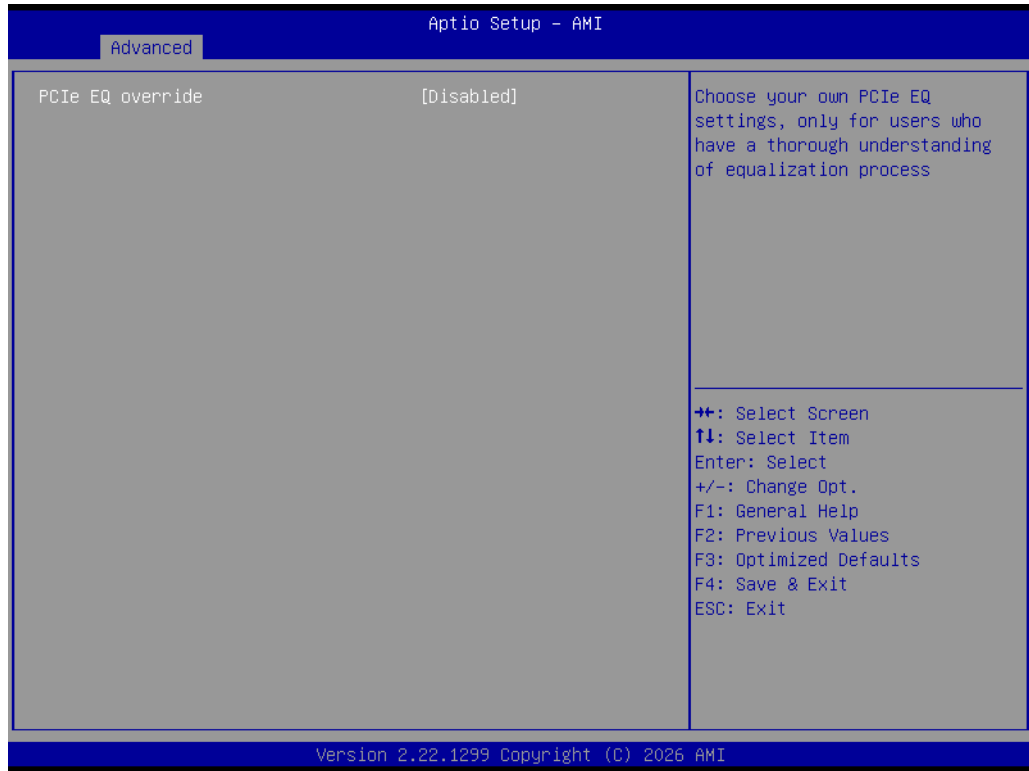
PCH Configuration

Advanced → PCIE Configuration → PCH Configuration

LAN1

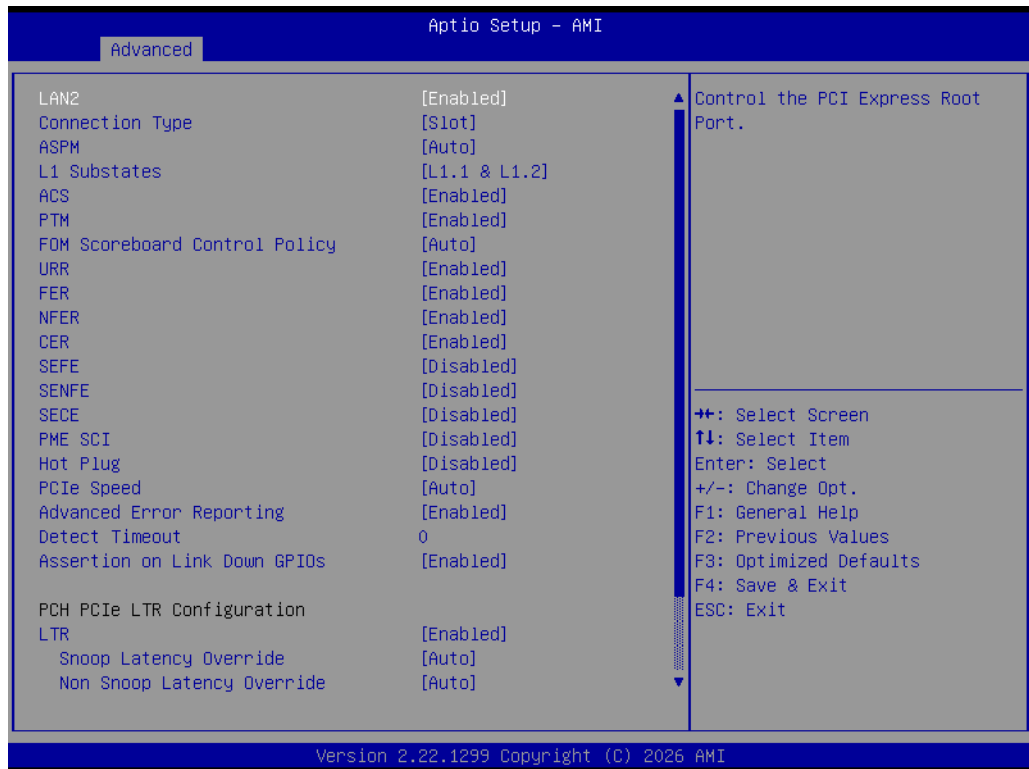
Advanced → PCIE Configuration → PCH Configuration → LAN1

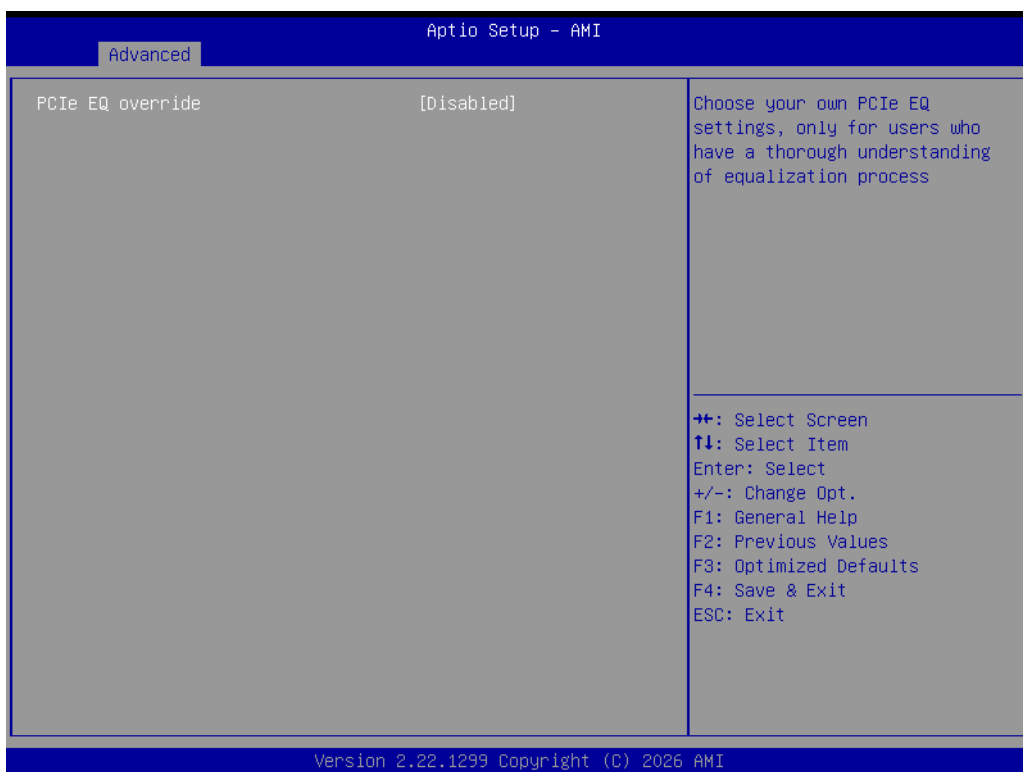
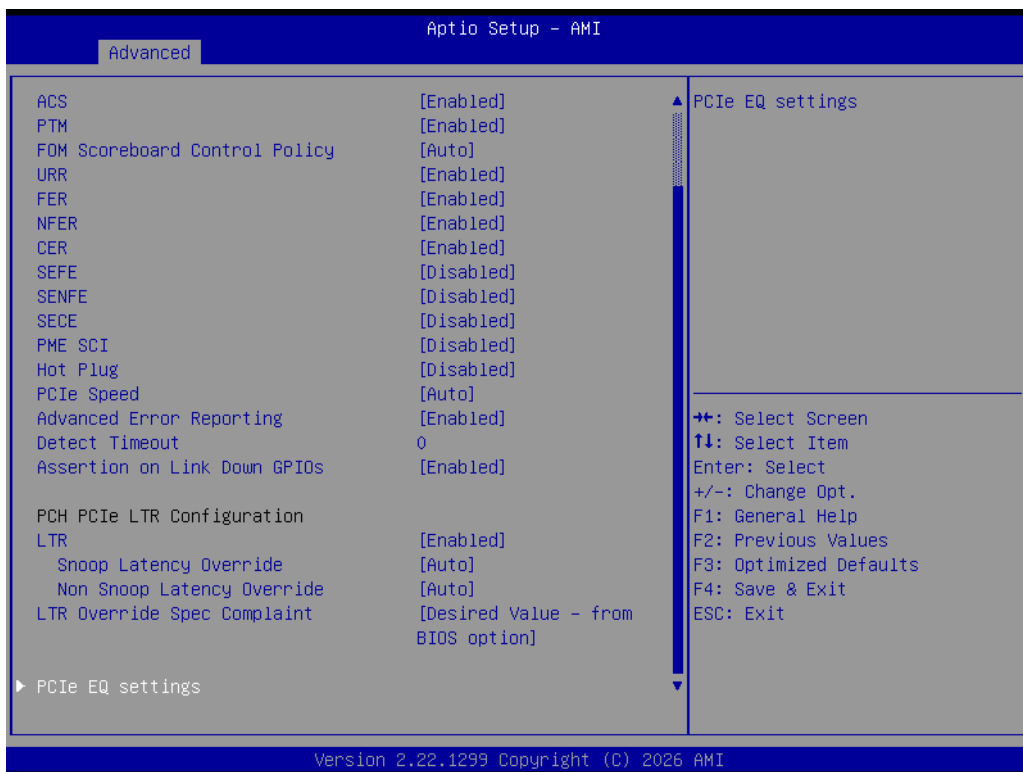




LAN2

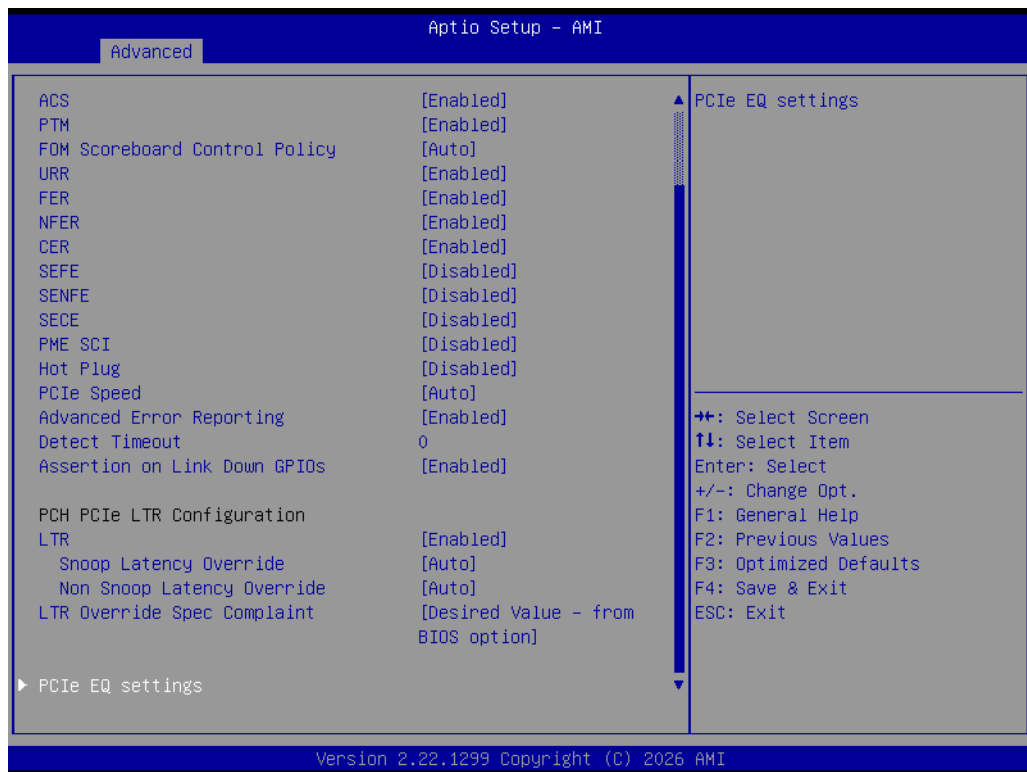
Advanced → PCIE Configuration → PCH Configuration → LAN2





LAN3

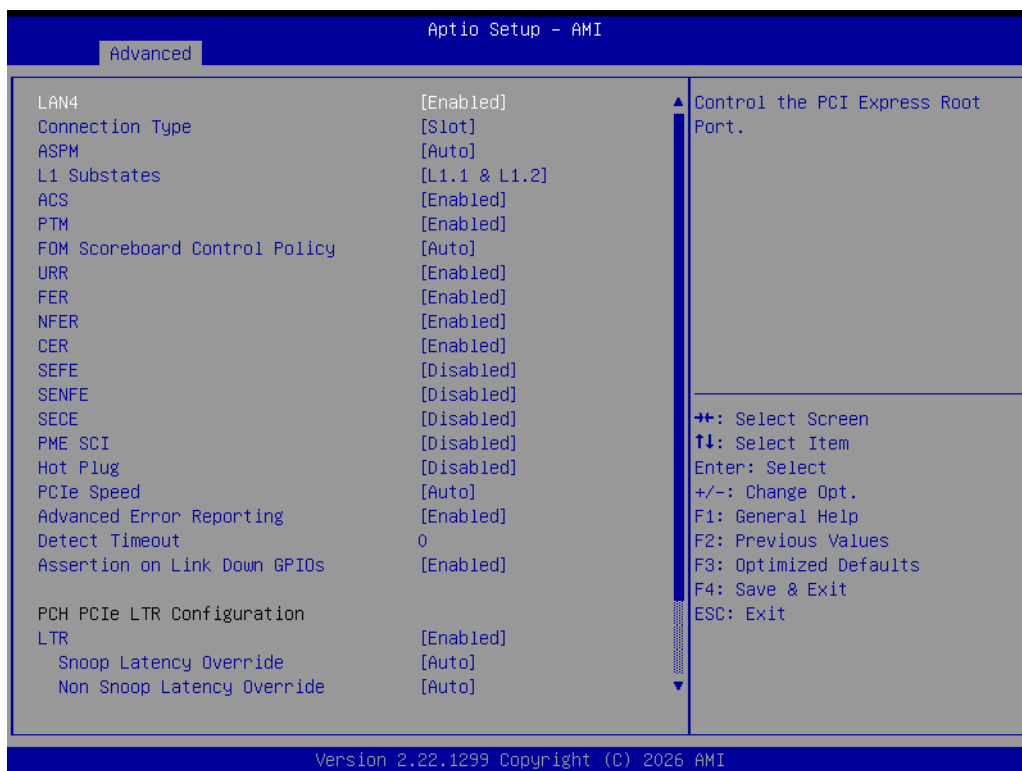
Advanced → PCIE Configuration → PCH Configuration → LAN3

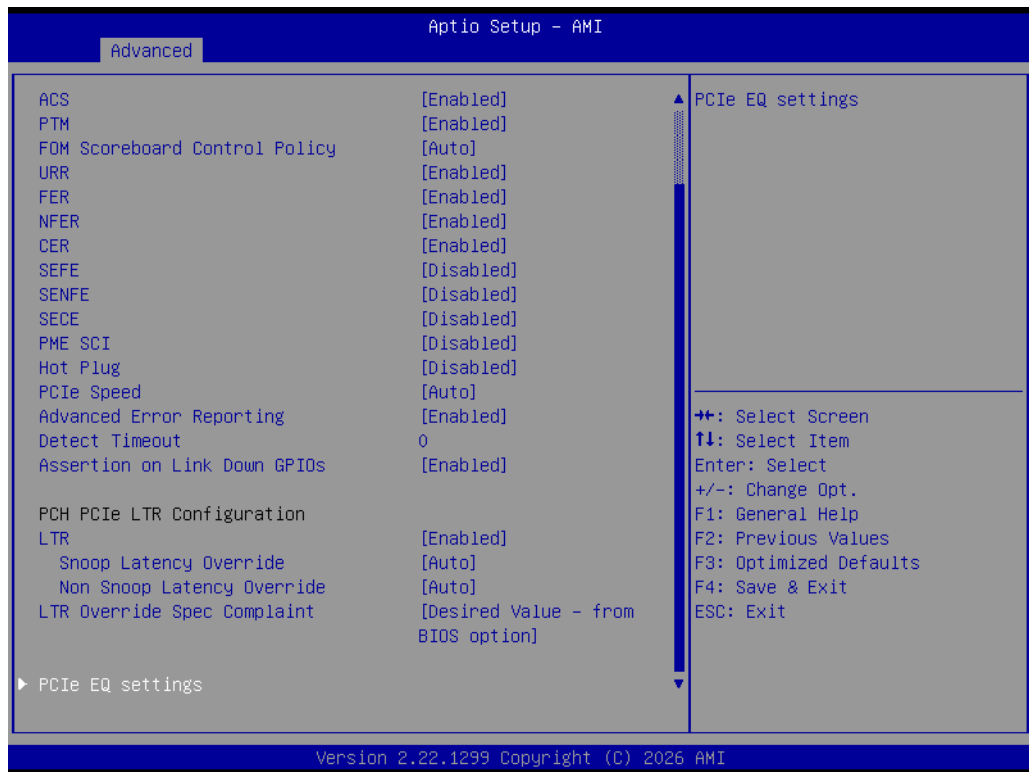




LAN4

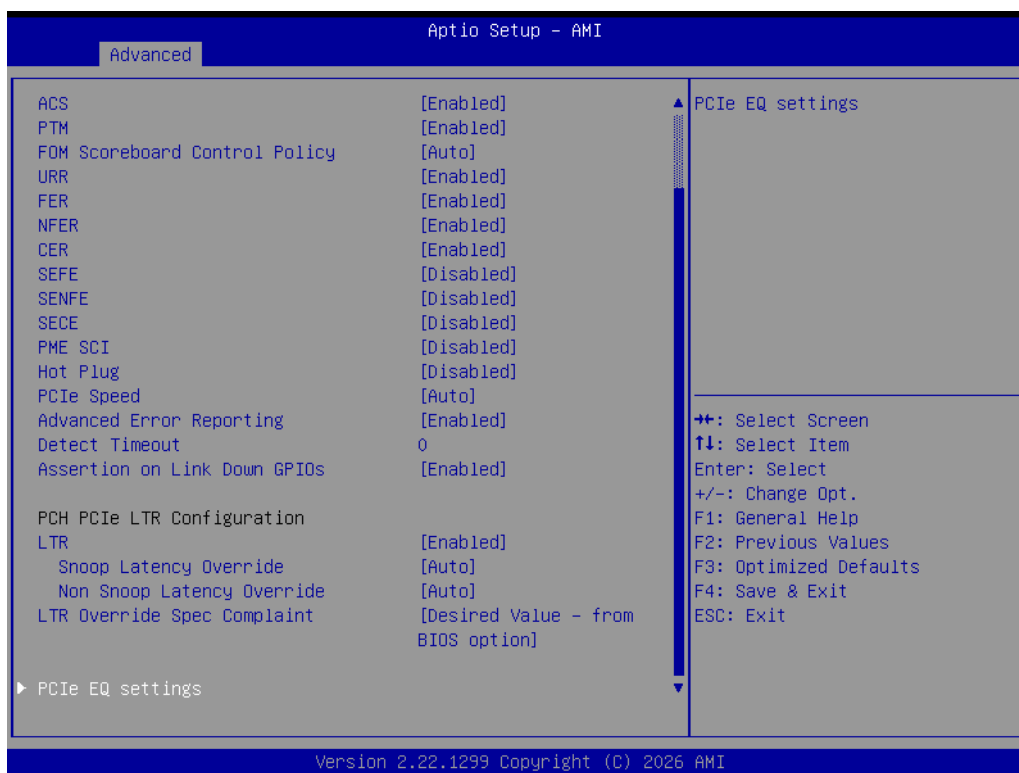
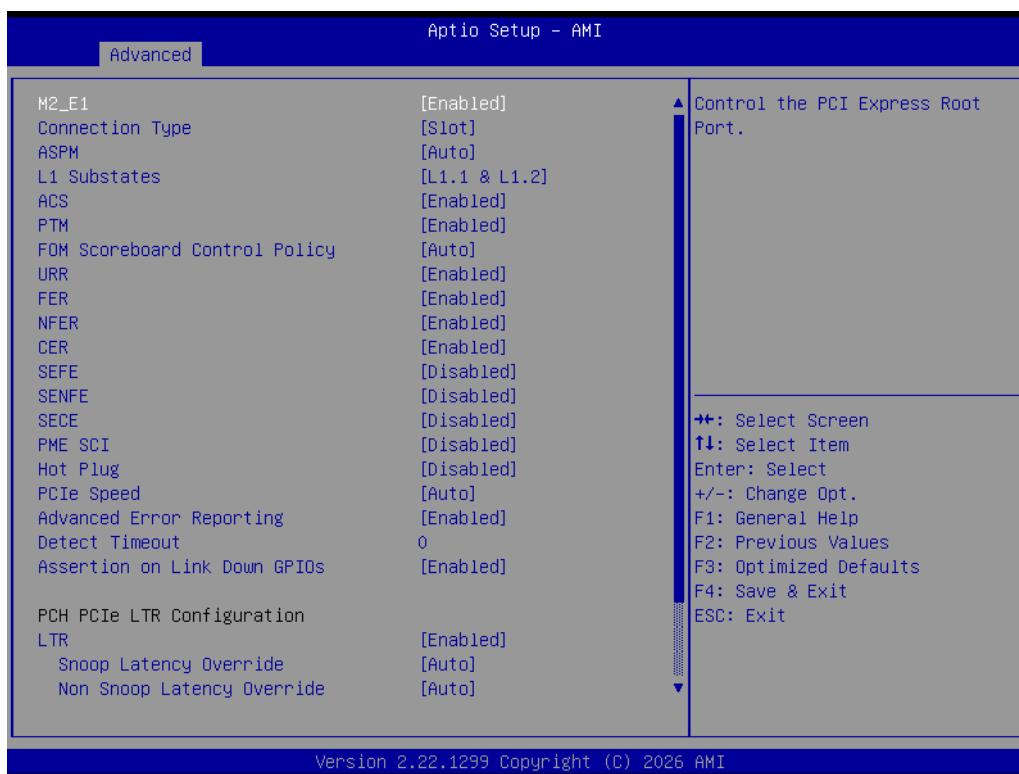
Advanced → PCIE Configuration → PCH Configuration → LAN4

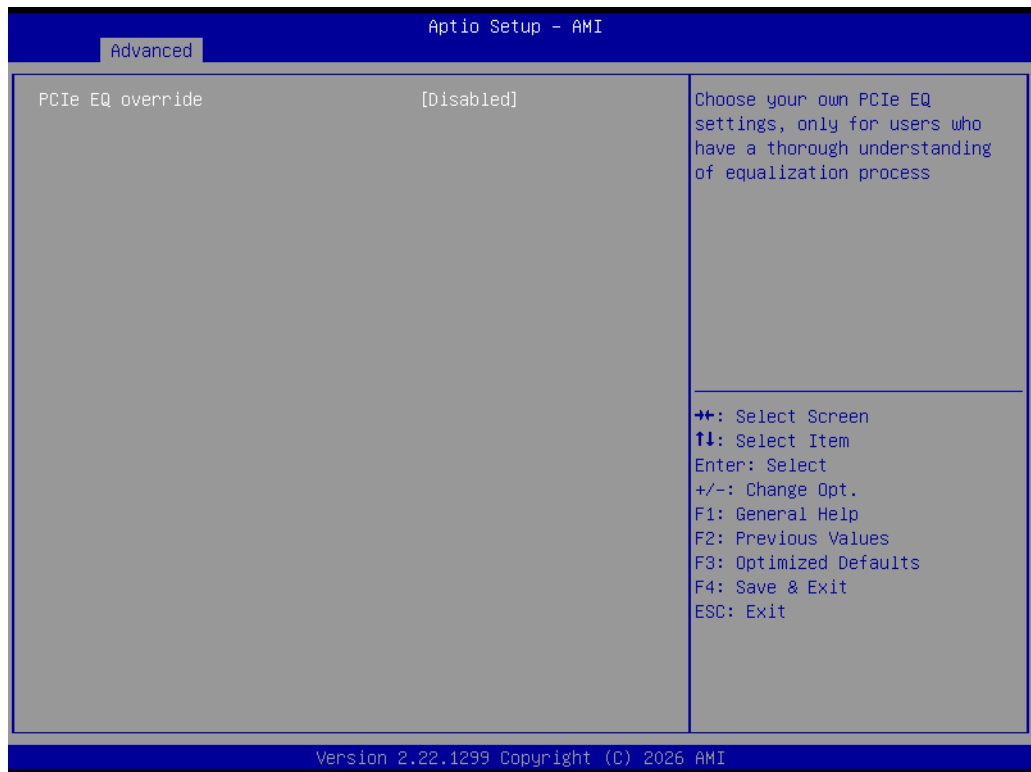




M.2 E-KEY

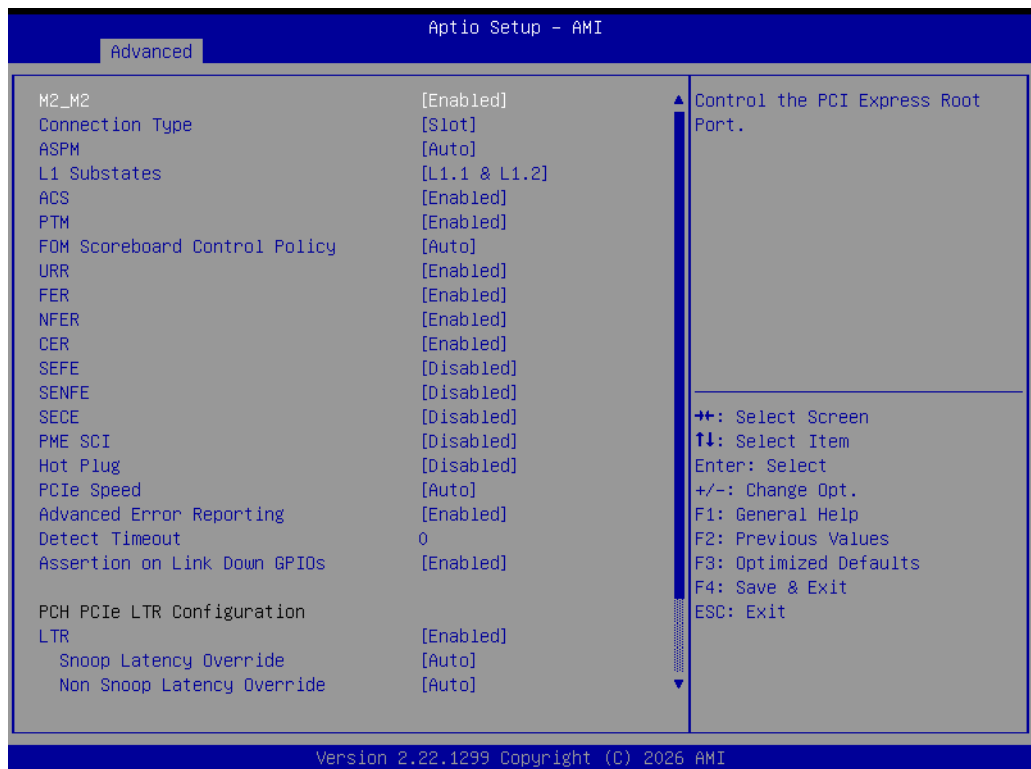
Advanced → PCIE Configuration → PCH Configuration → M.2 E-KEY

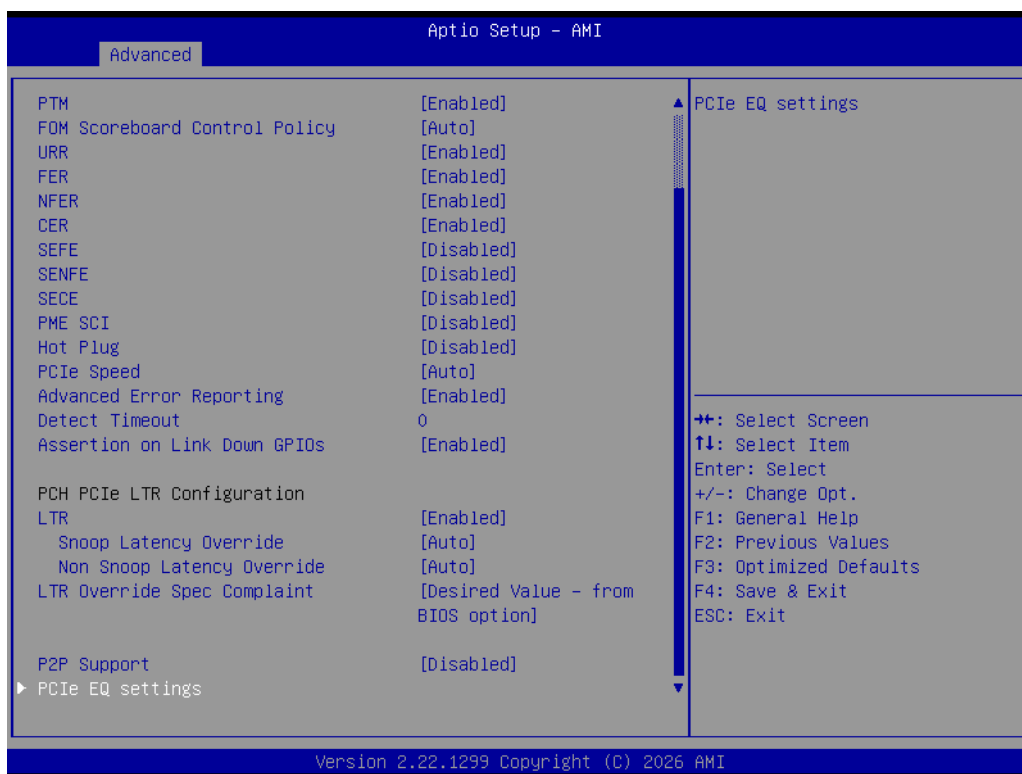




M.2 M-KEY

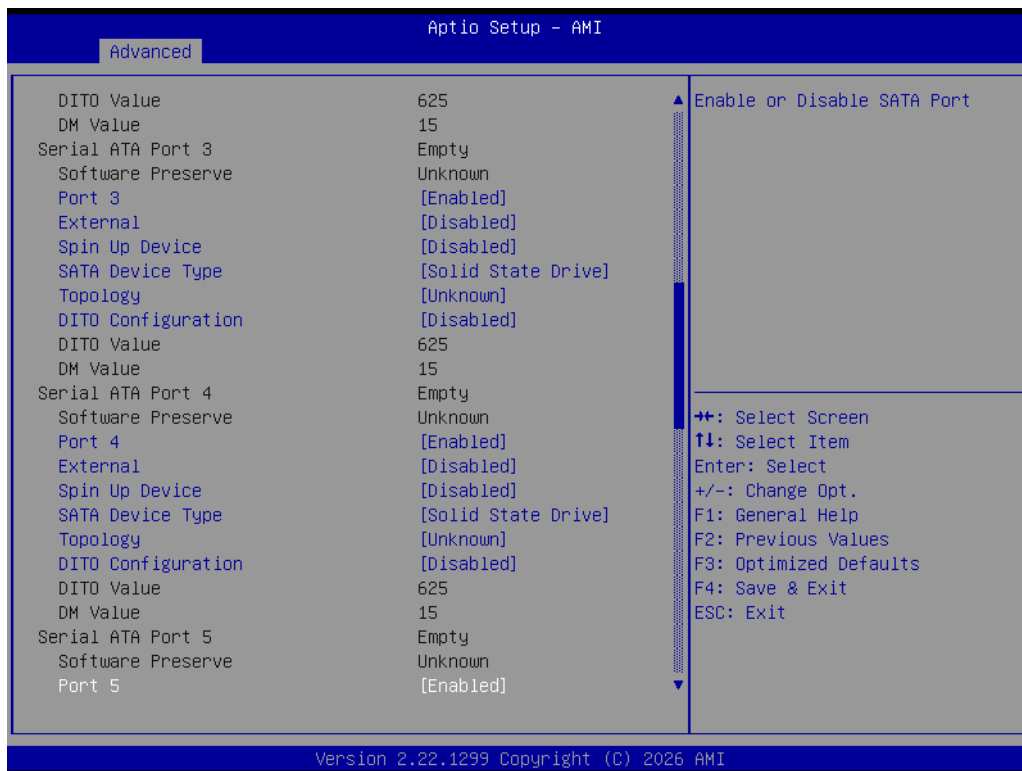
Advanced → PCIE Configuration → PCH Configuration → M.2 M-KEY





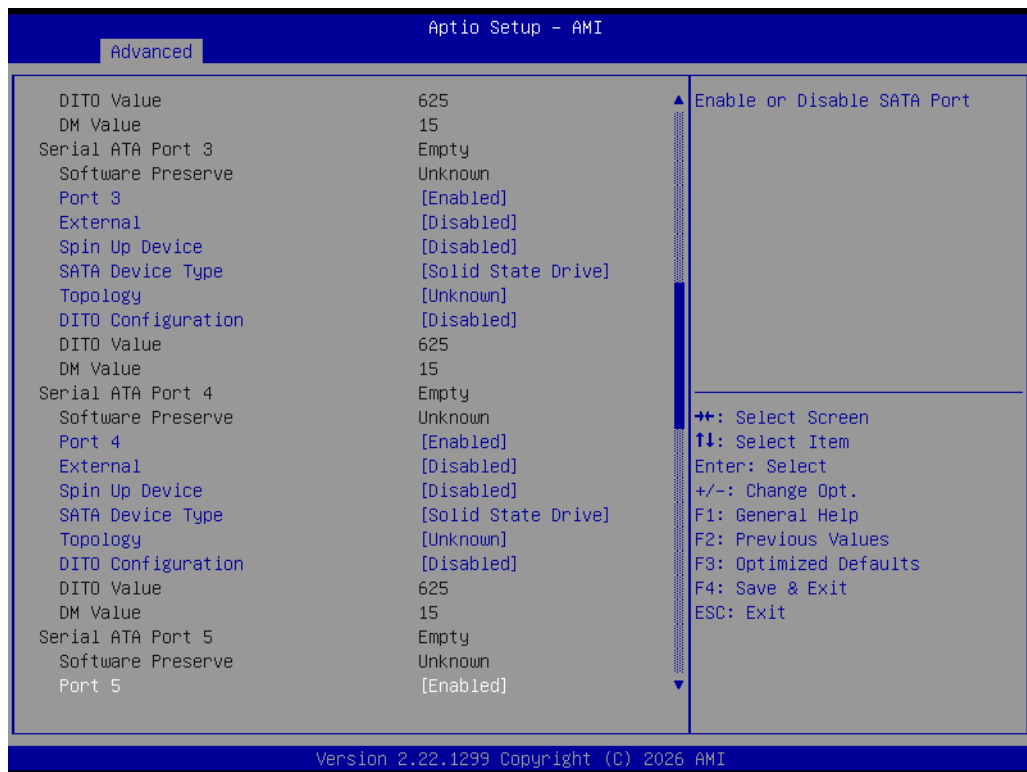
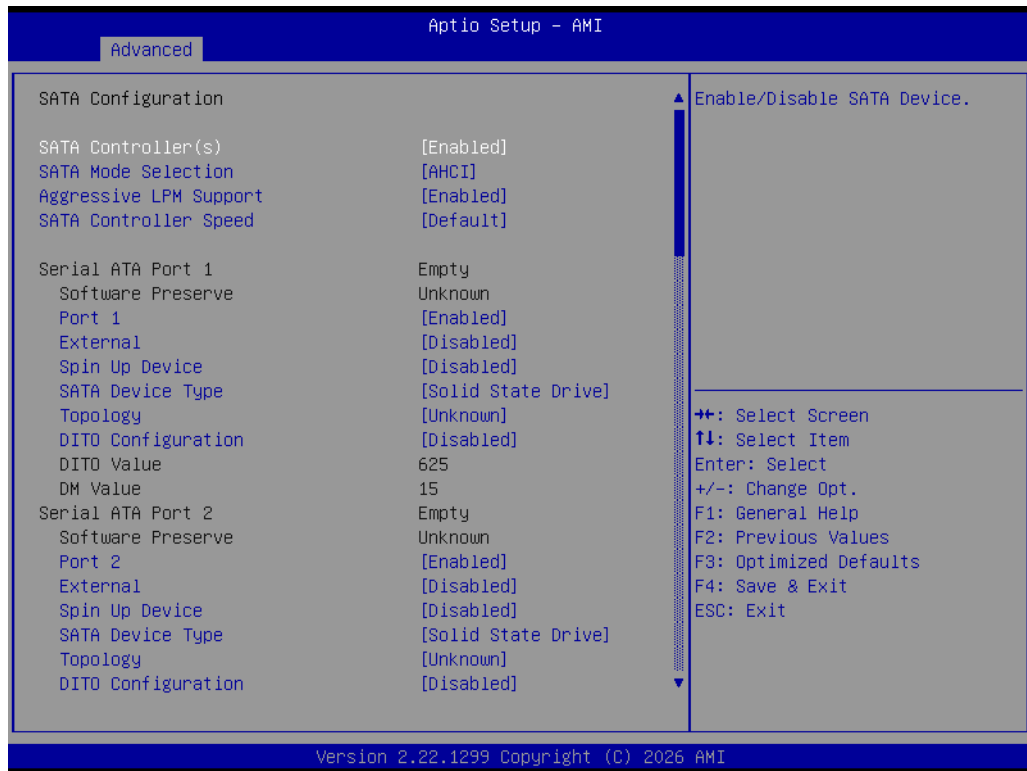
3.2.2.5 PCH-IO Configuration

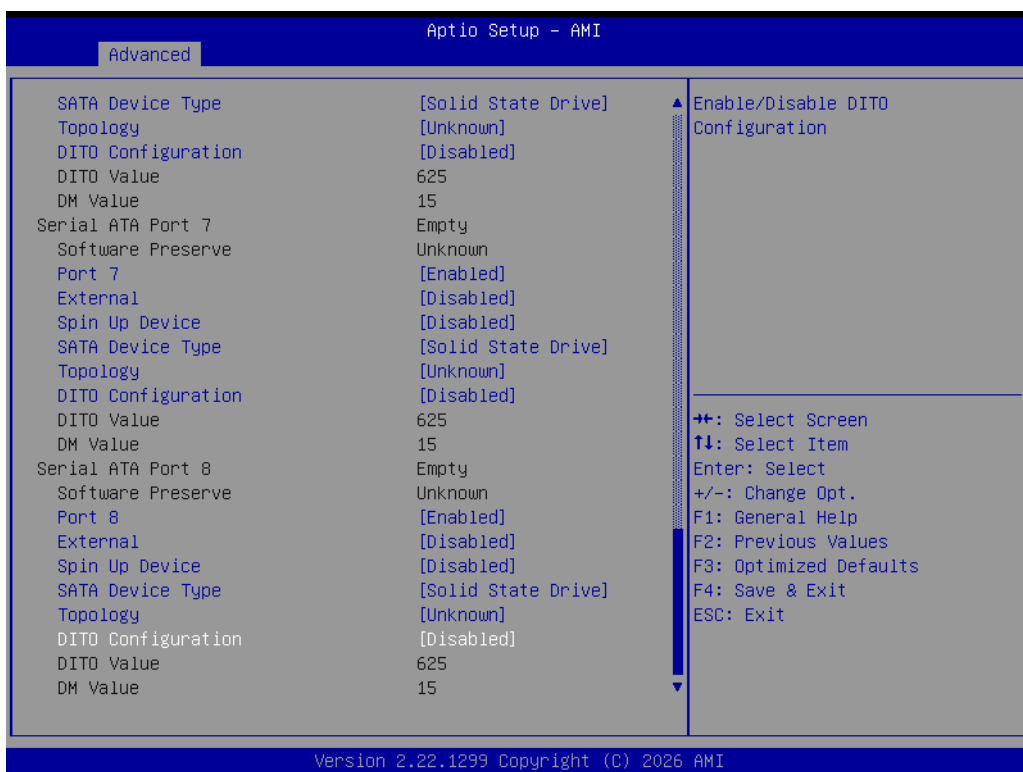
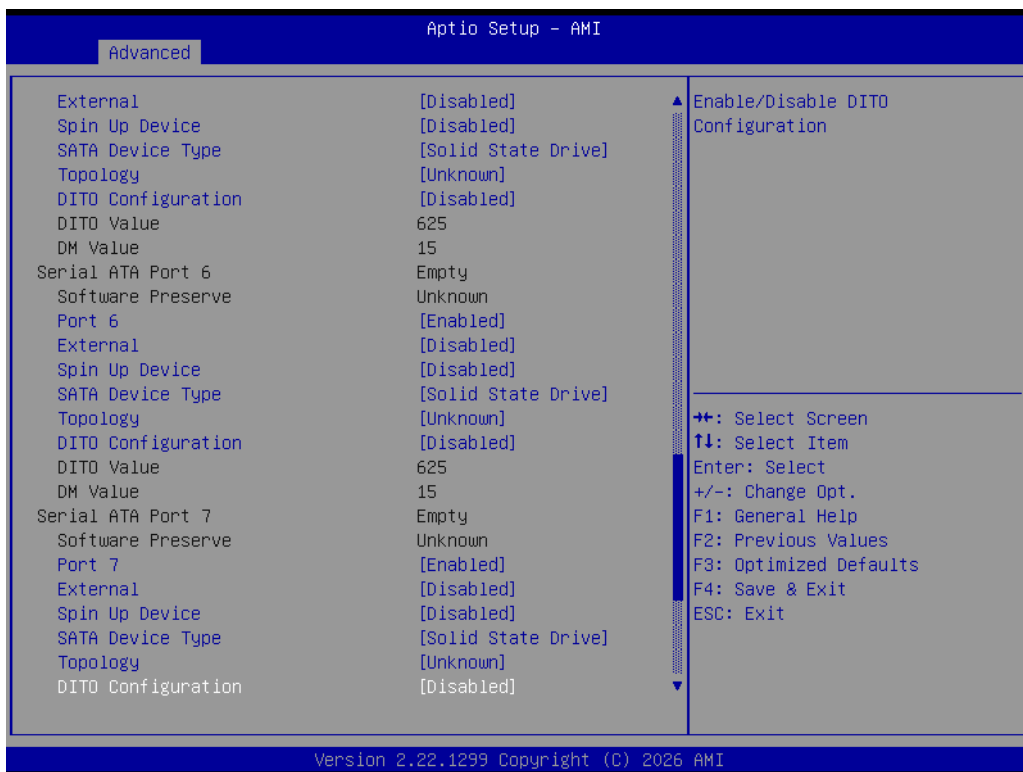
Advanced → PCH-IO Configuration



SATA Configuration

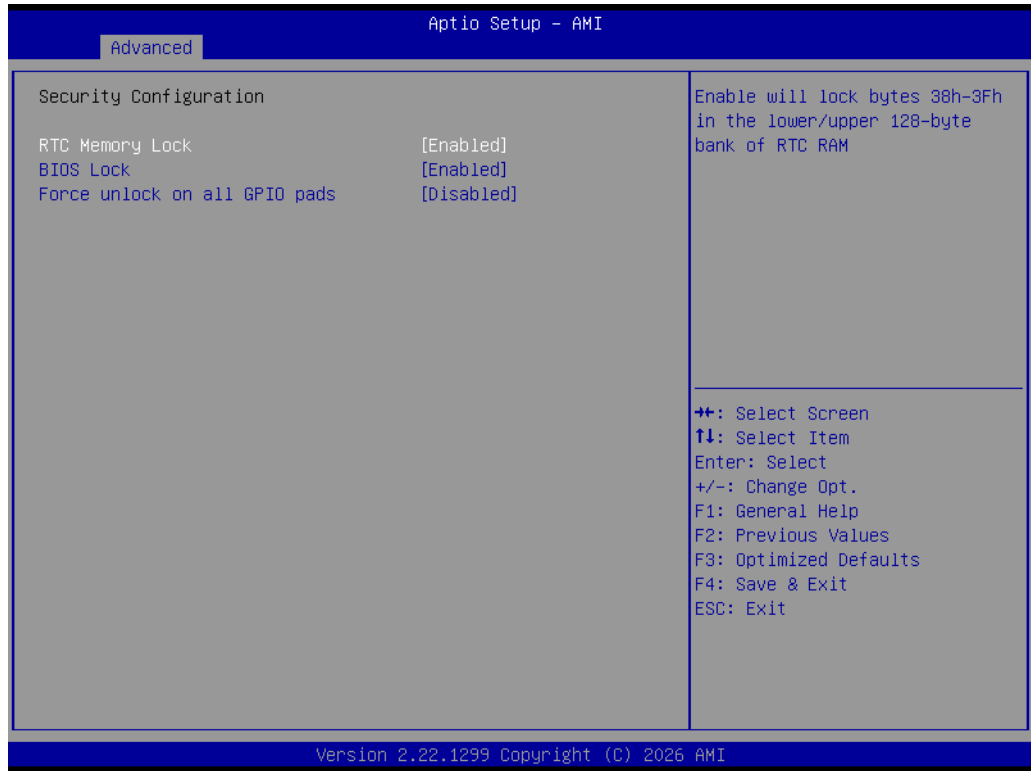
Advanced → PCH-IO Configuration → SATA Configuration





Security Configuration

Advanced → PCH-IO Configuration → Security Configuration



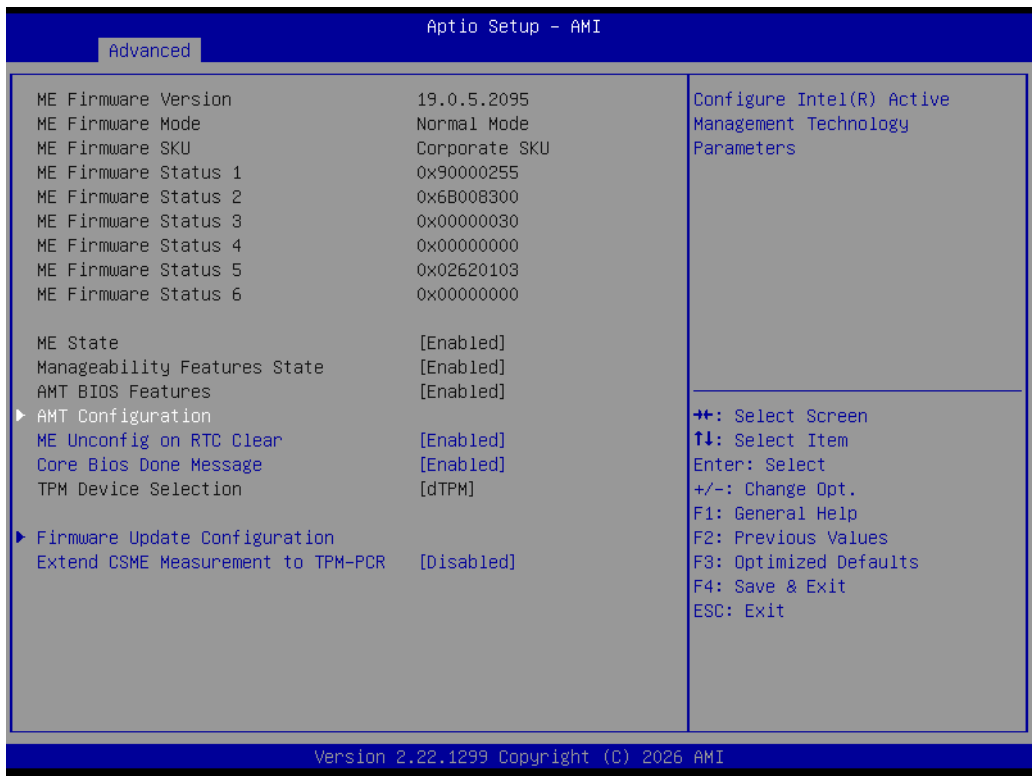
HD Audio Subsystem Configuration Settings

Advanced → PCH-IO Configuration → HD Audio Subsystem Configuration Settings



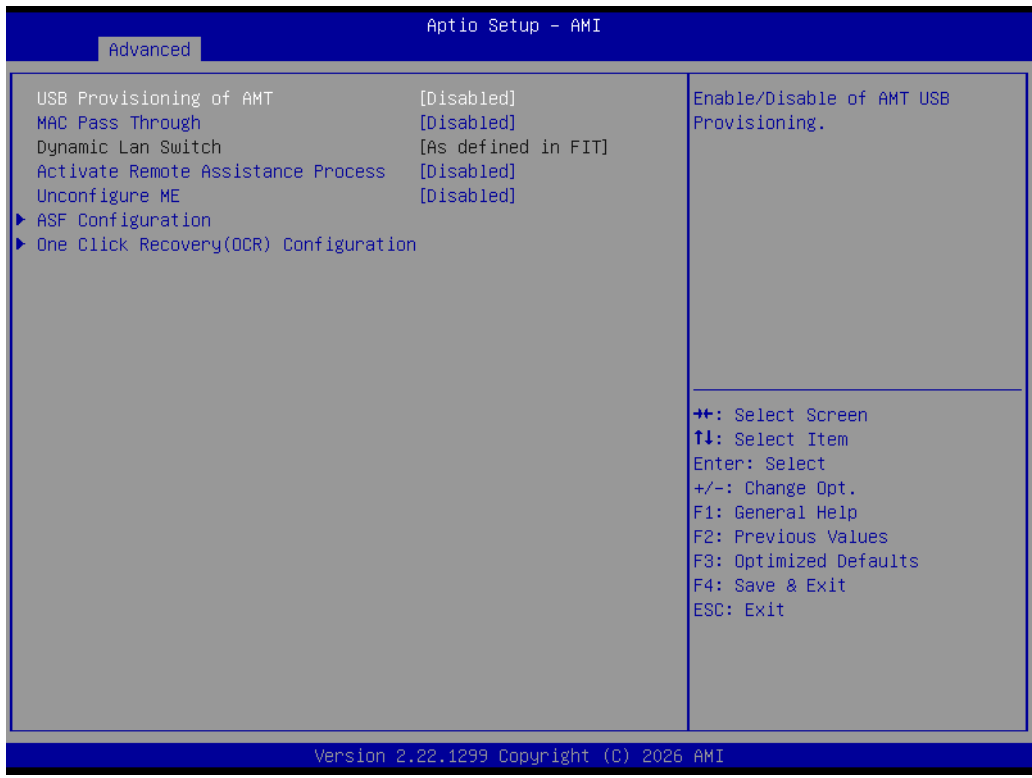
3.2.2.6 PCH-FW Configuration

Advanced → PCH-FW Configuration



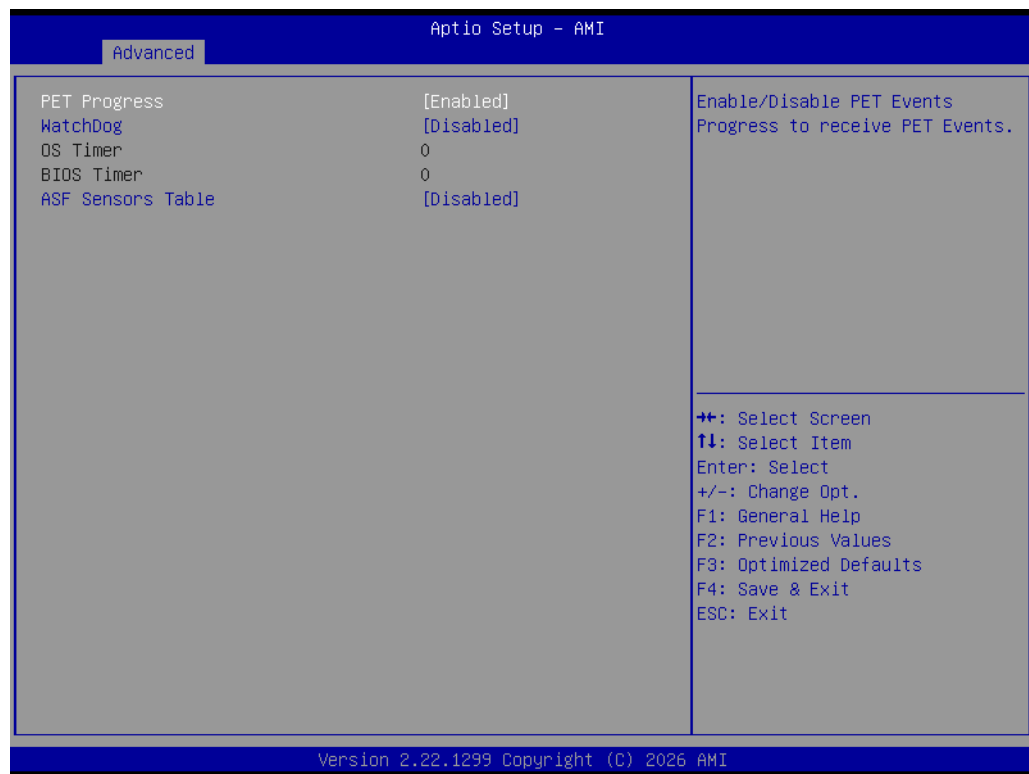
AMT Configuration

Advanced → PCH-FW Configuration → AMT Configuration



ASF Configuration

Advanced → PCH-FW Configuration → AMT Configuration → ASF Configuration



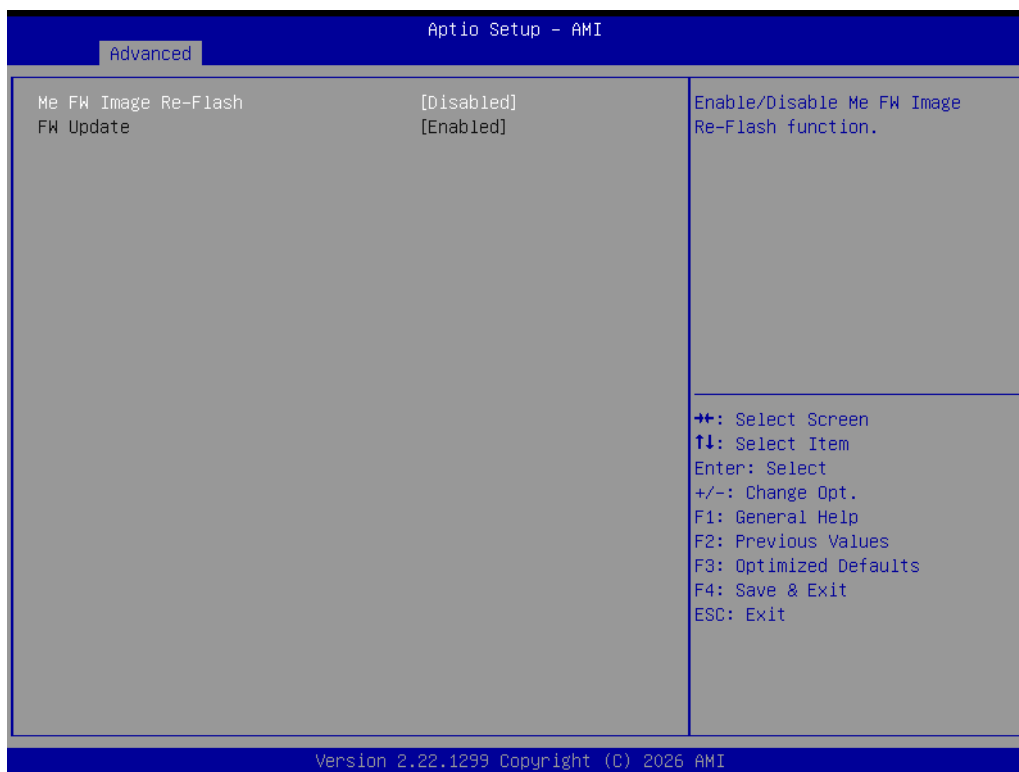
One Click Recovery (OCR) Configuration

Advanced → PCH-FW Configuration → AMT Configuration → One Click Recovery (OCR) Configuration



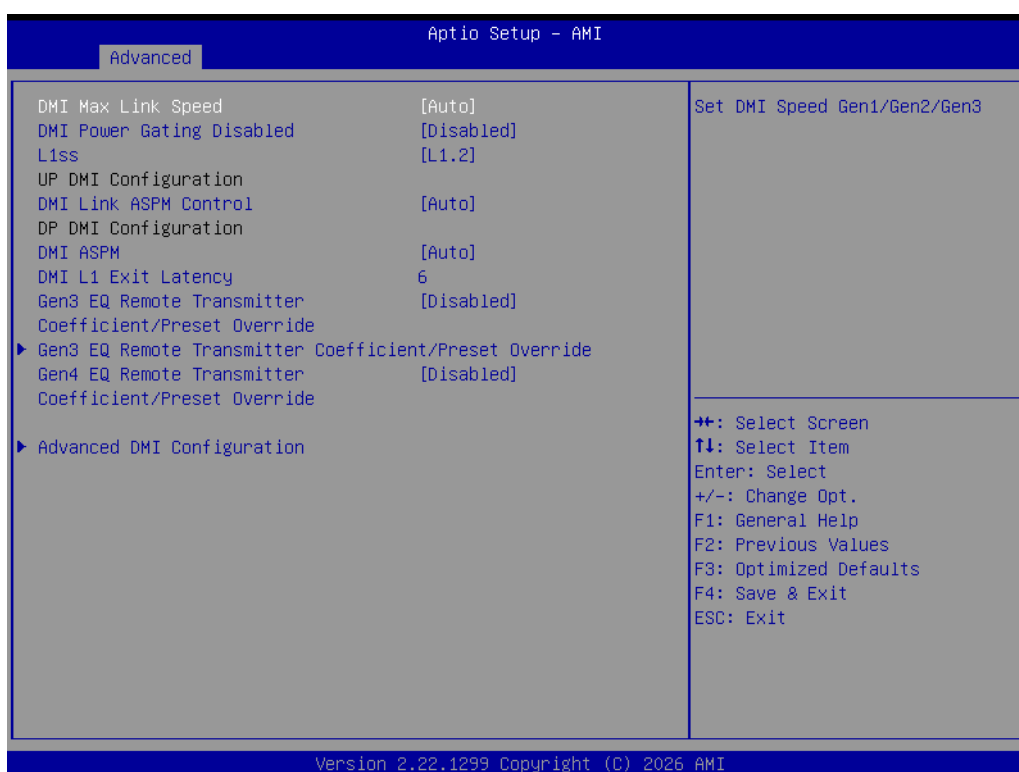
Firmware Update Configuration

Advanced → PCH-FW Configuration → Firmware Update Configuration



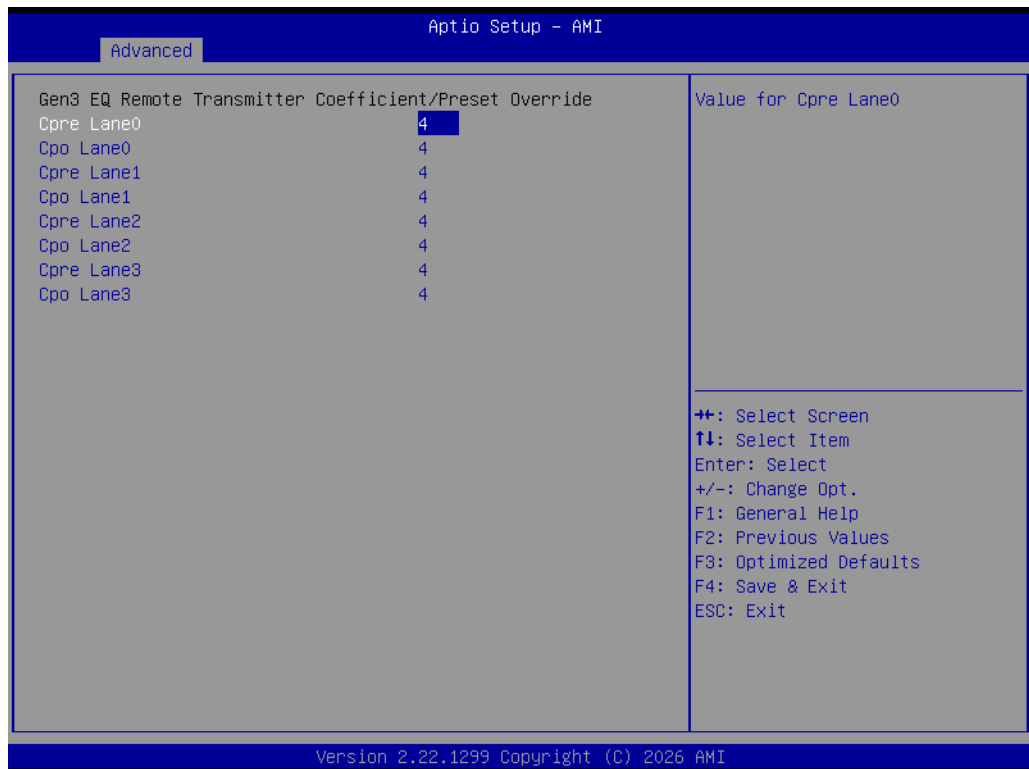
3.2.2.7 DMI Configuration

Advanced → DMI Configuration



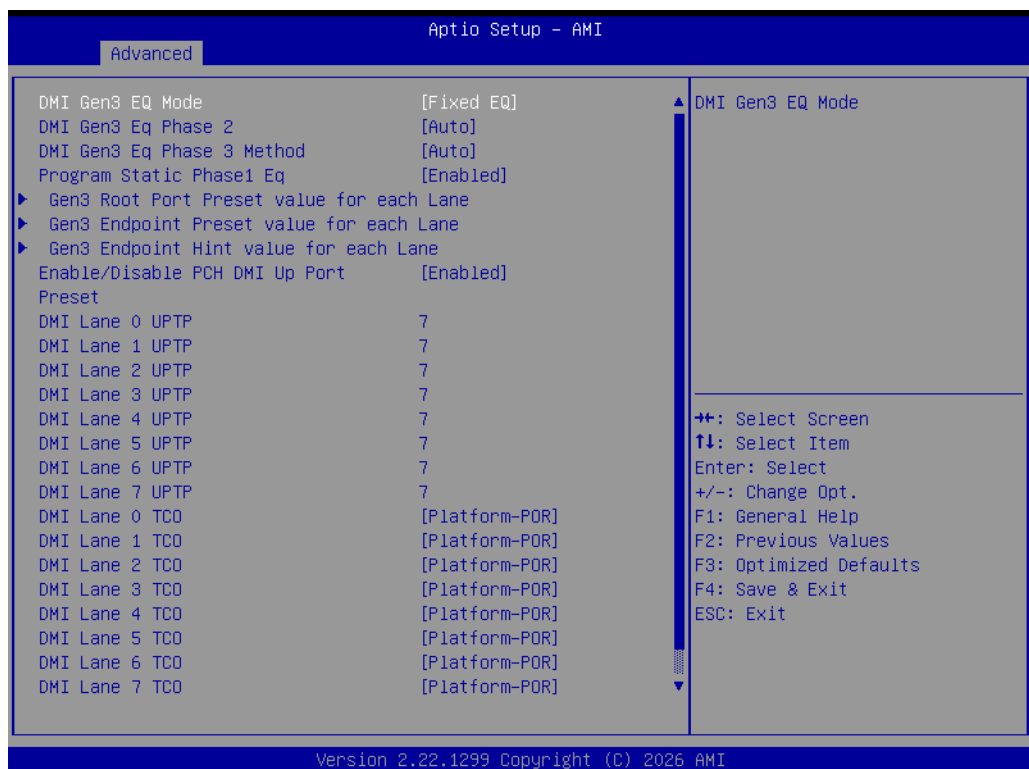
Gen3 EQ Remote Transmitter Coefficient/Preset Override

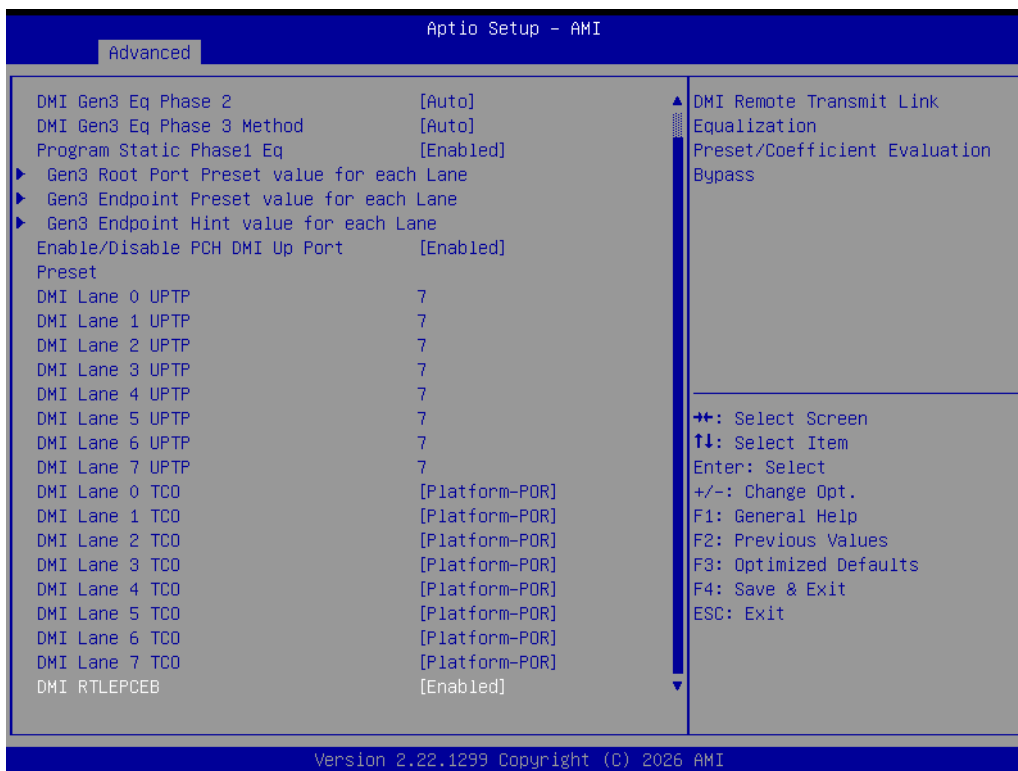
Advanced → DMI Configuration → Gen3 EQ Remote Transmitter Coefficient/Preset Override



Advanced DMI Configuration

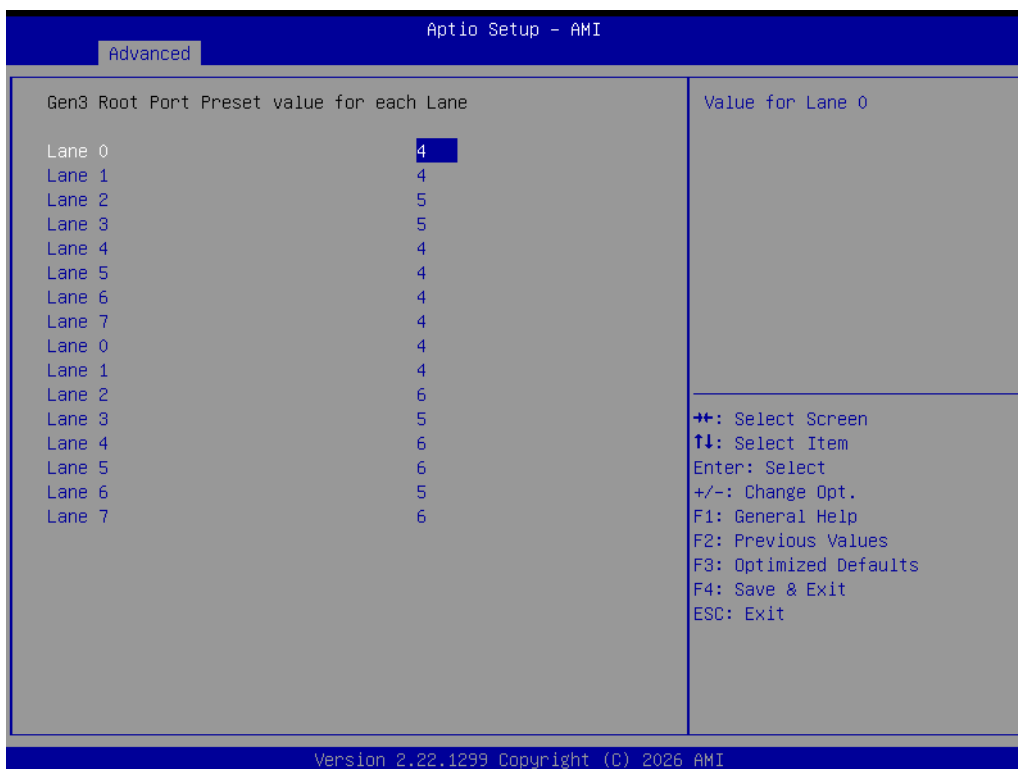
Advanced → DMI Configuration → Advanced DMI Configuration





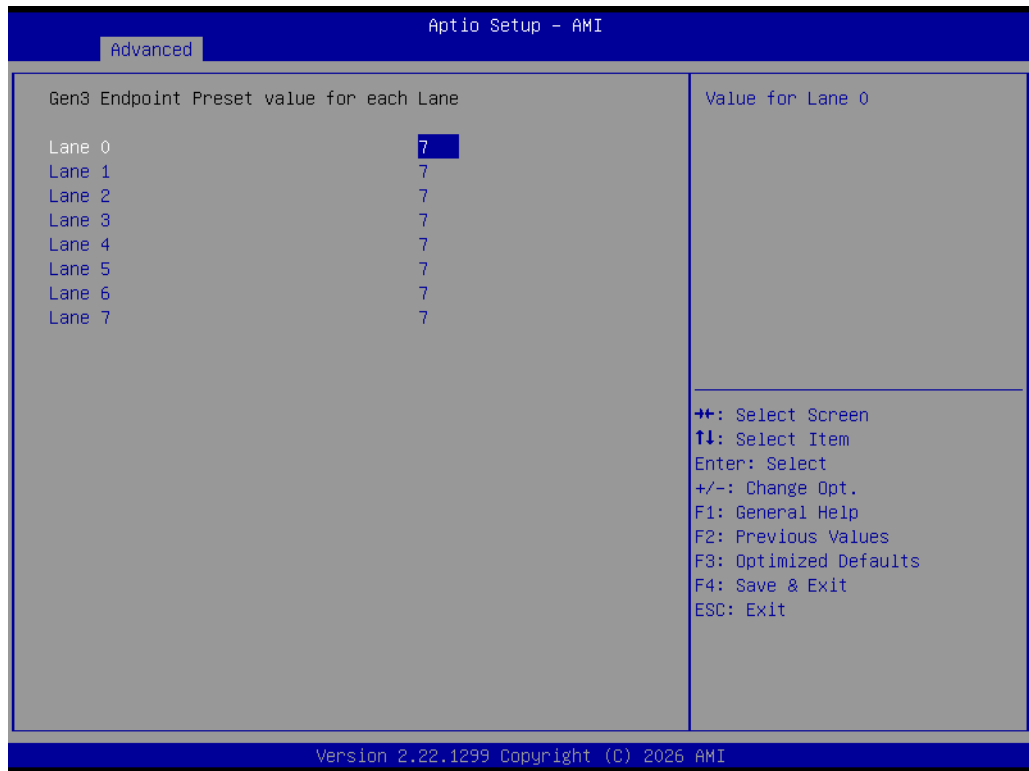
Gen3 Root Port Preset value for each Lane

Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Root Port Preset value for each Lane



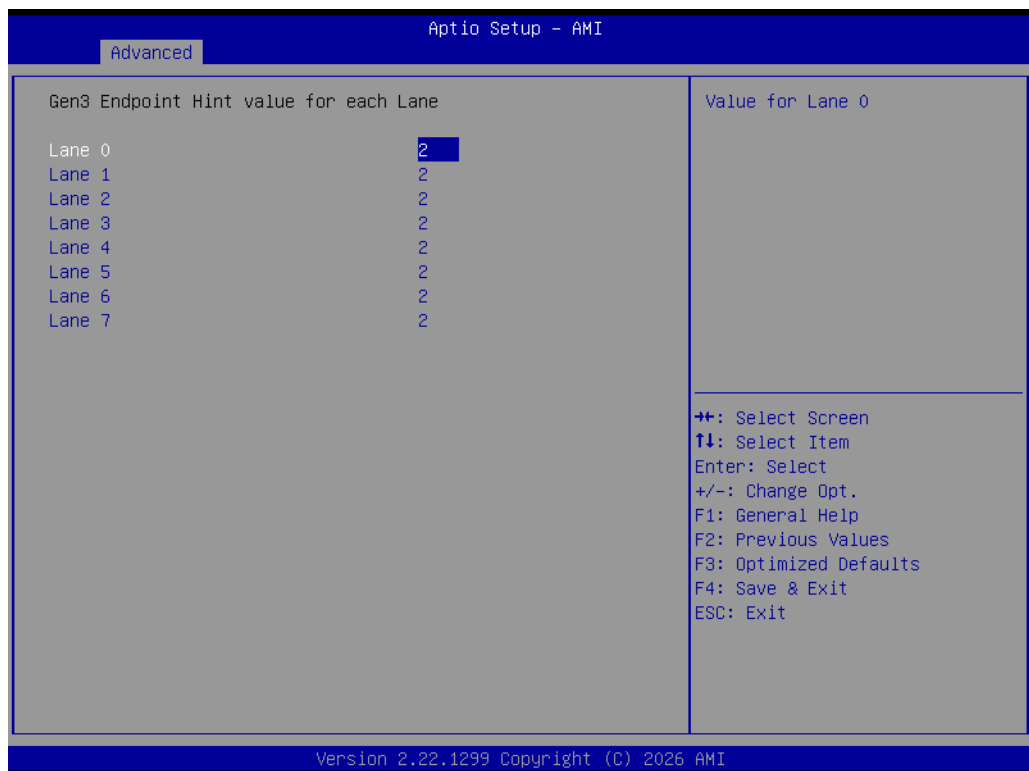
Gen3 Endpoint Preset value for each Lane

Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Endpoint Preset value for each Lane



Gen3 Endpoint Hint value for each Lane

Advanced → DMI Configuration → Advanced DMI Configuration → Gen3 Endpoint Hint value for each Lane



3.2.2.8 Trusted Computing

Advanced → Trusted Computing



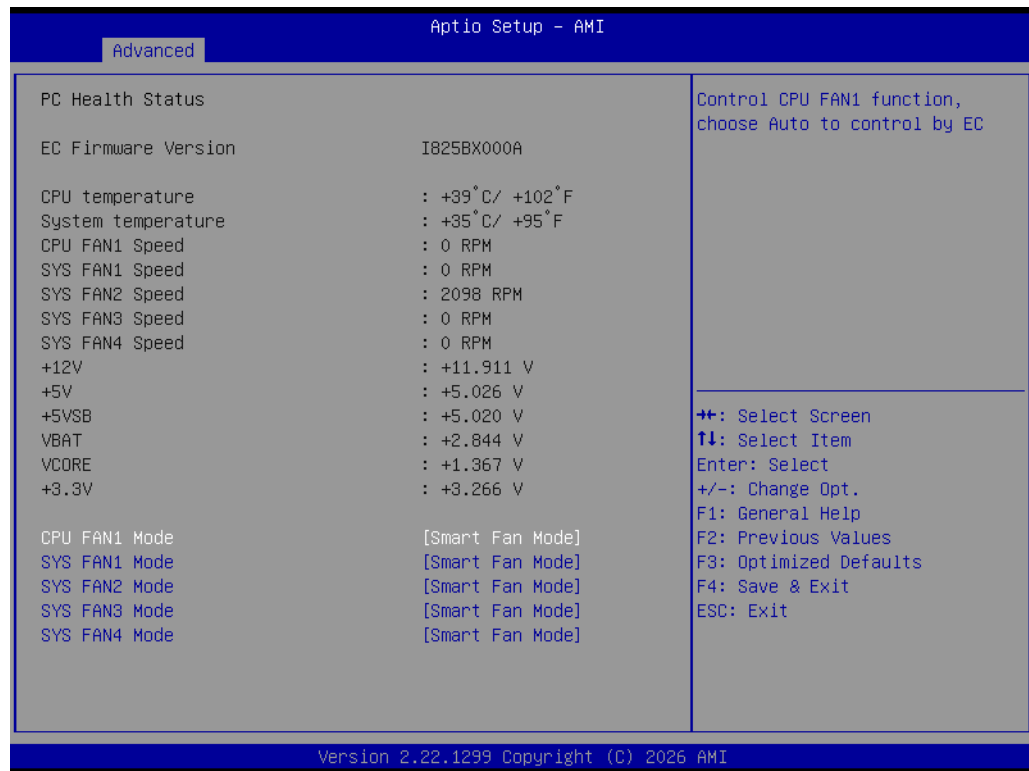
3.2.2.9 ACPI Settings

Advanced → ACPI Settings



3.2.2.10 IT5782 HW Monitor

Advanced → IT5782 HW Monitor



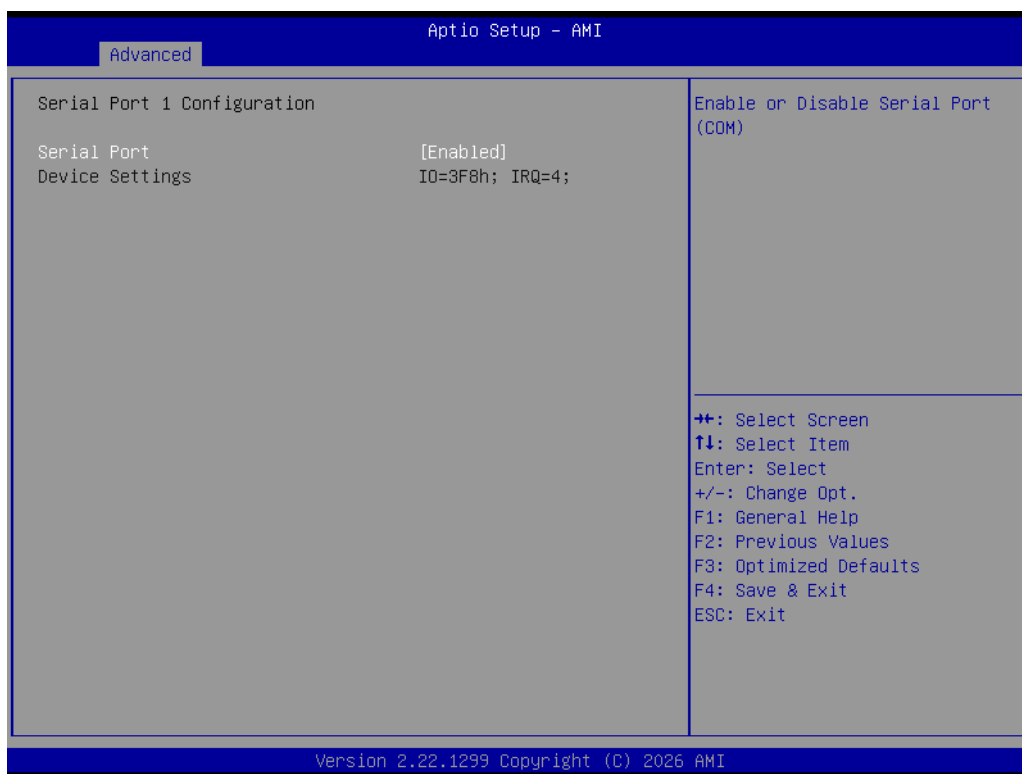
3.2.2.11 IT5782 Embedded Controller Configuration

Advanced → IT5782 Embedded Controller Configuration



Serial Port 1 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 1 Configuration



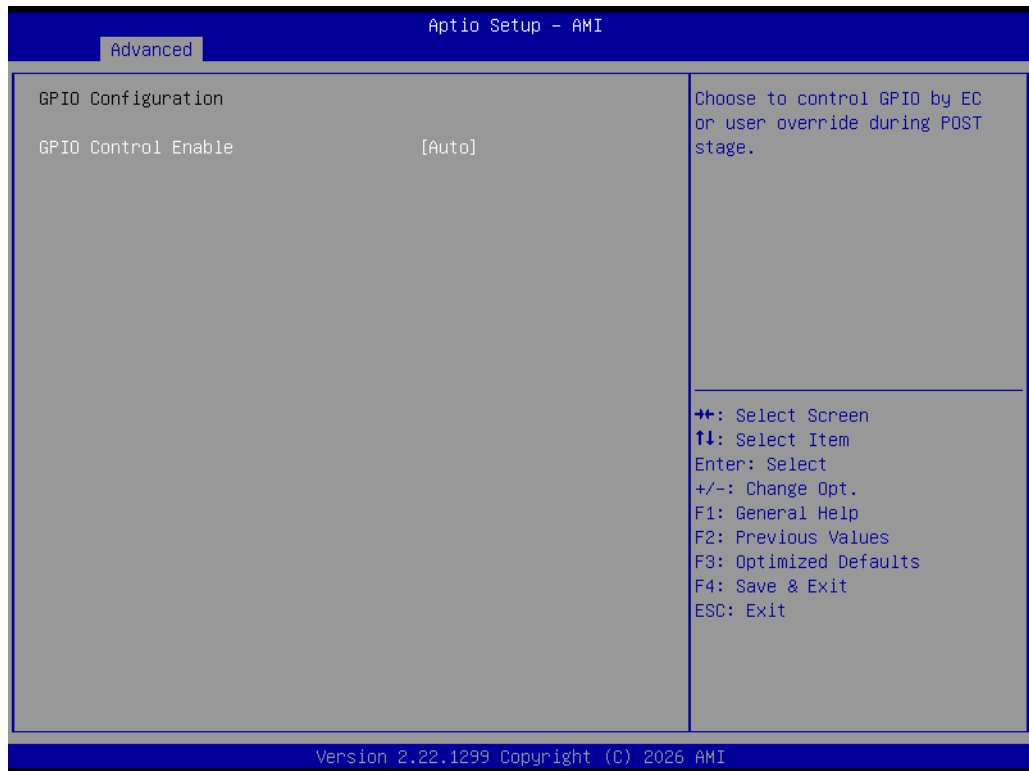
Serial Port 2 Configuration

Advanced → IT5782 Embedded Controller Configuration → Serial Port 2 Configuration



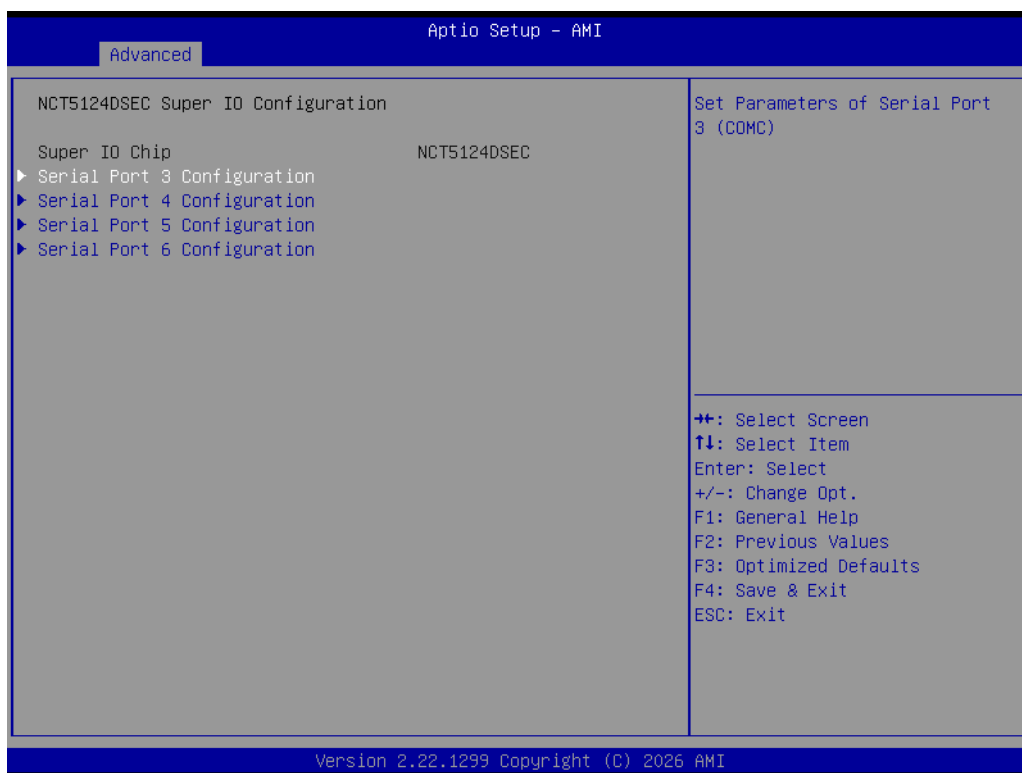
GPIO Configuration

Advanced → IT5782 Embedded Controller Configuration → GPIO Configuration



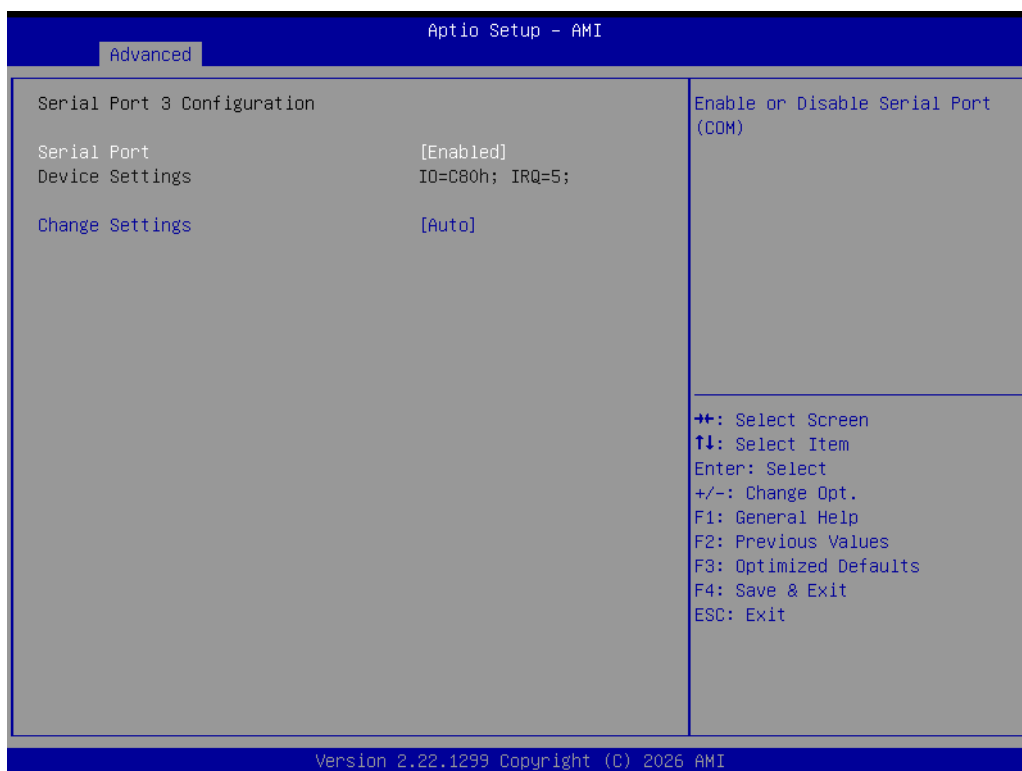
3.2.2.12 NCT5124DSEC Super IO Configuration

Advanced → NCT5124DSEC Super IO Configuration



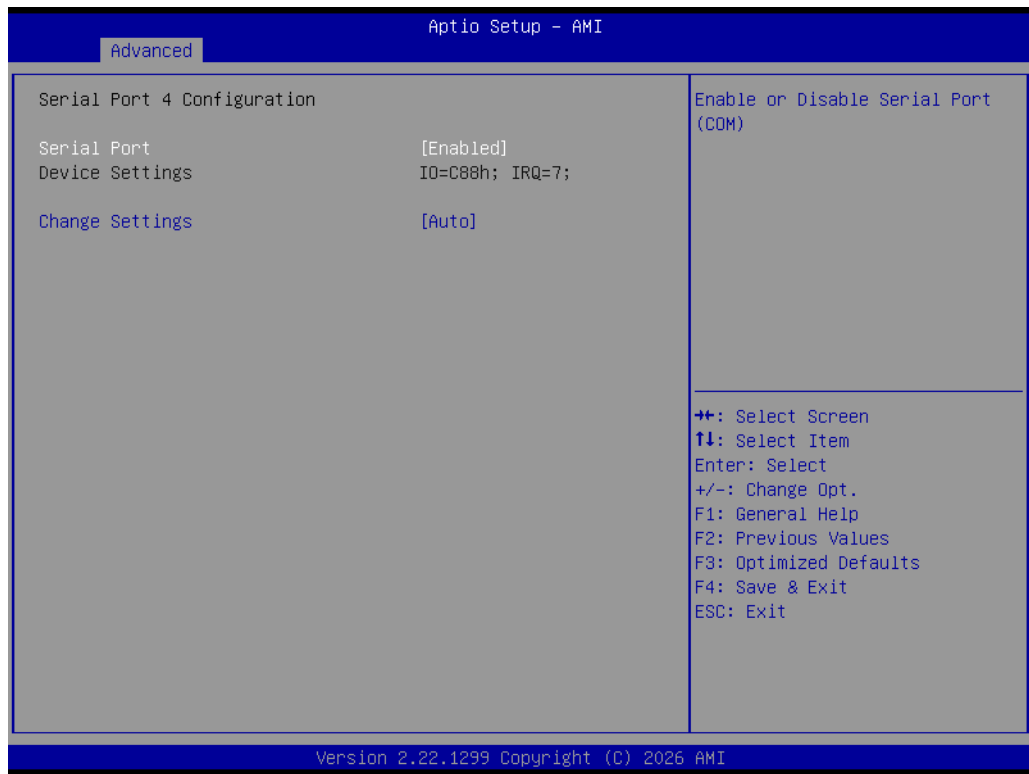
Serial Port 3 Configuration

Advanced → NCT5124DSEC Super IO Configuration → Serial Port 3 Configuration



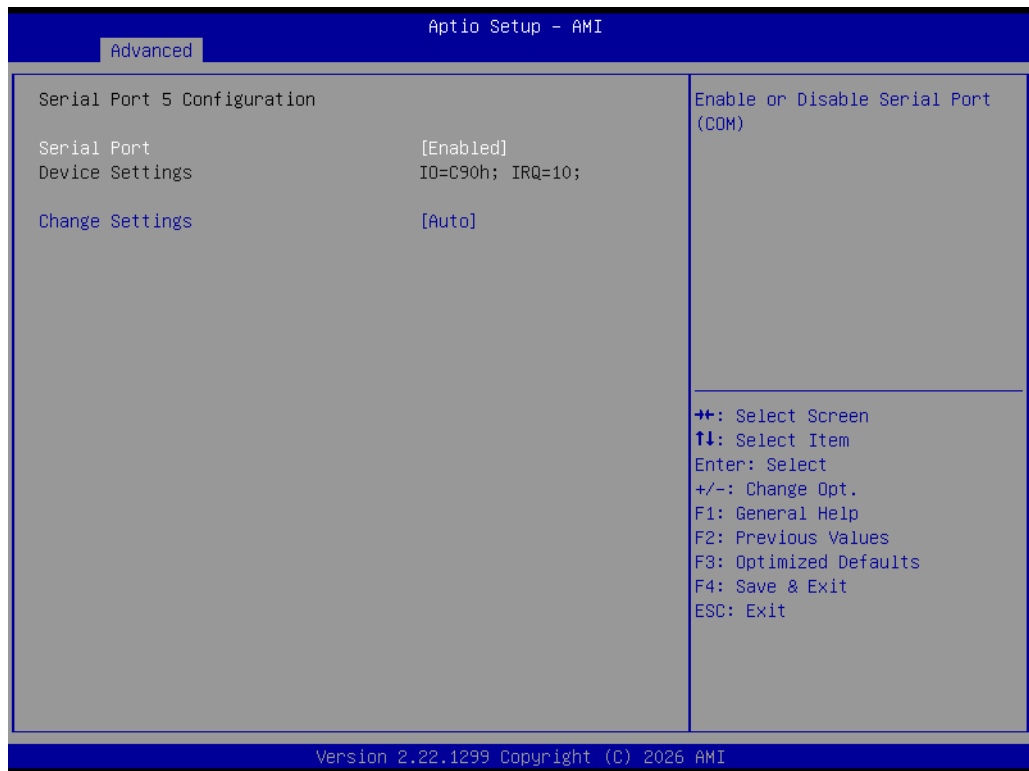
Serial Port 4 Configuration

Advanced → NCT5124DSEC Super IO Configuration → Serial Port 4 Configuration



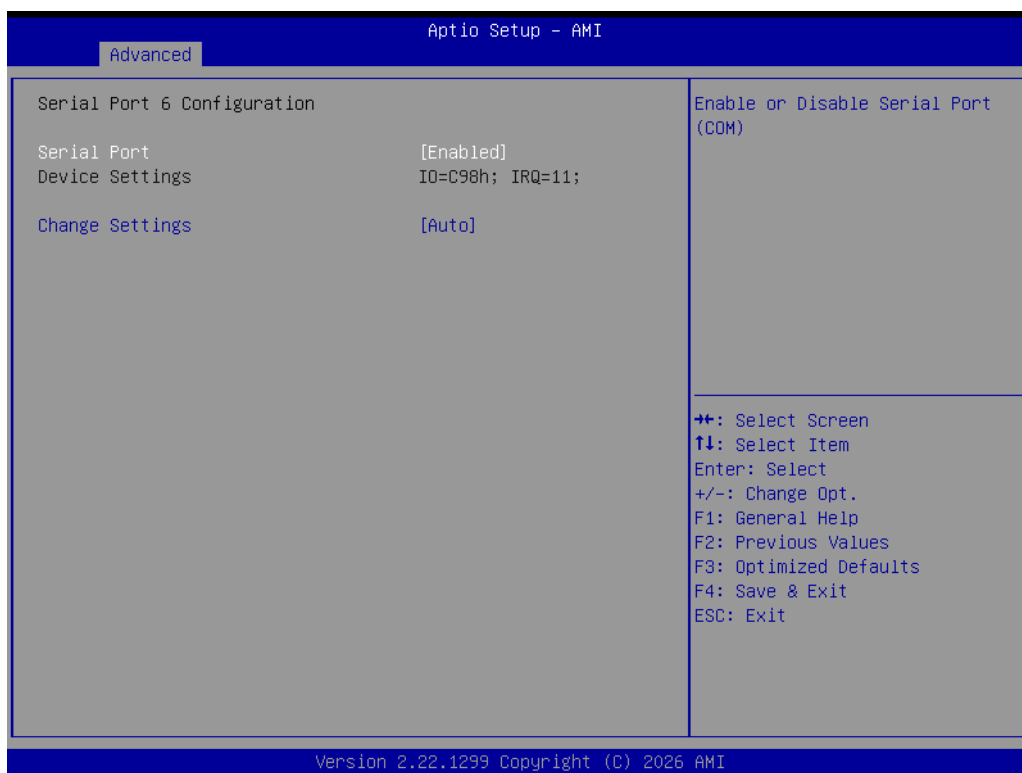
Serial Port 5 Configuration

Advanced → NCT5124DSEC Super IO Configuration → Serial Port 5 Configuration



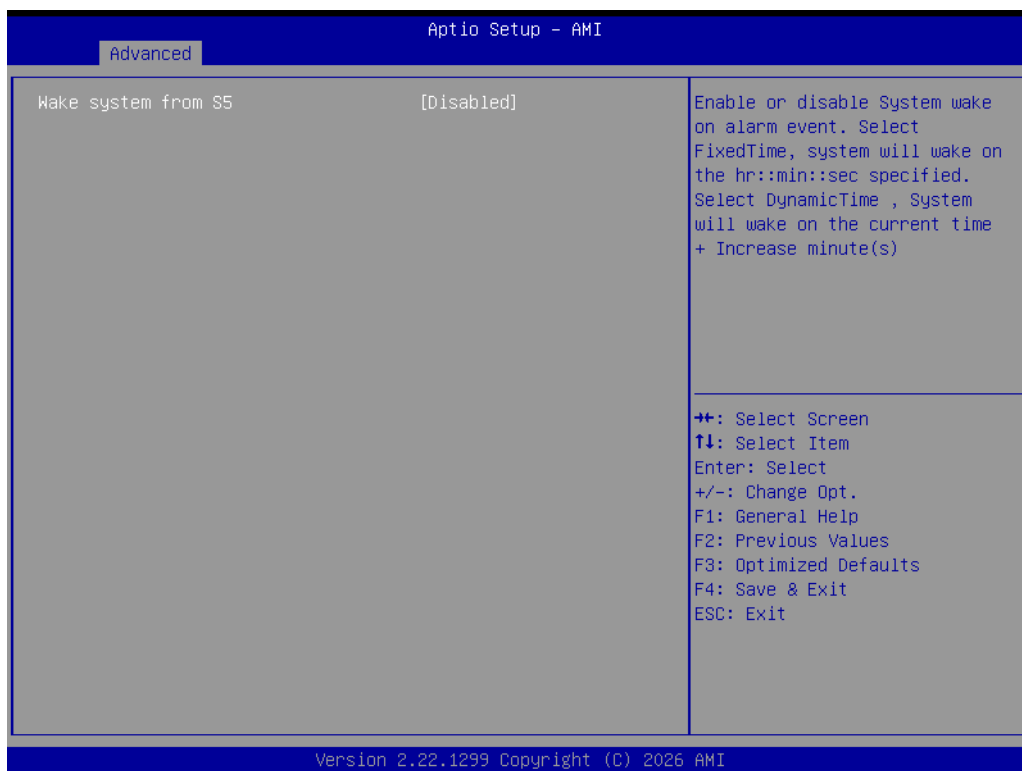
Serial Port 6 Configuration

Advanced → NCT5124DSEC Super IO Configuration → Serial Port 6 Configuration



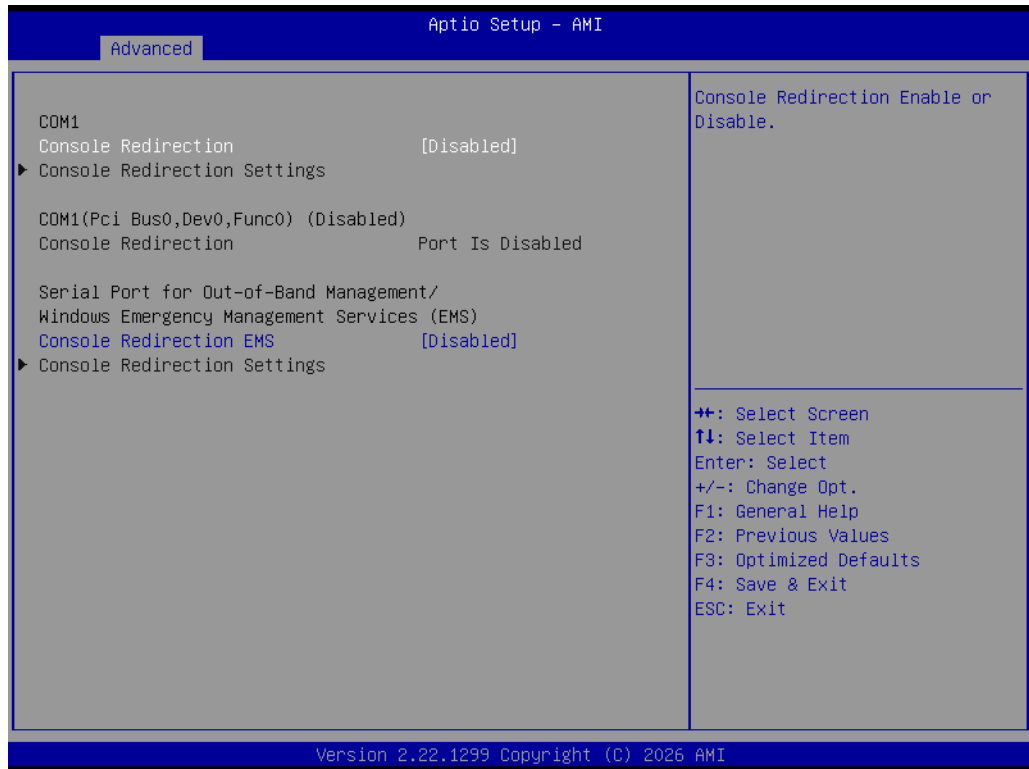
3.2.2.13 S5 RTC Wake Settings

Advanced → S5 RTC Wake Settings



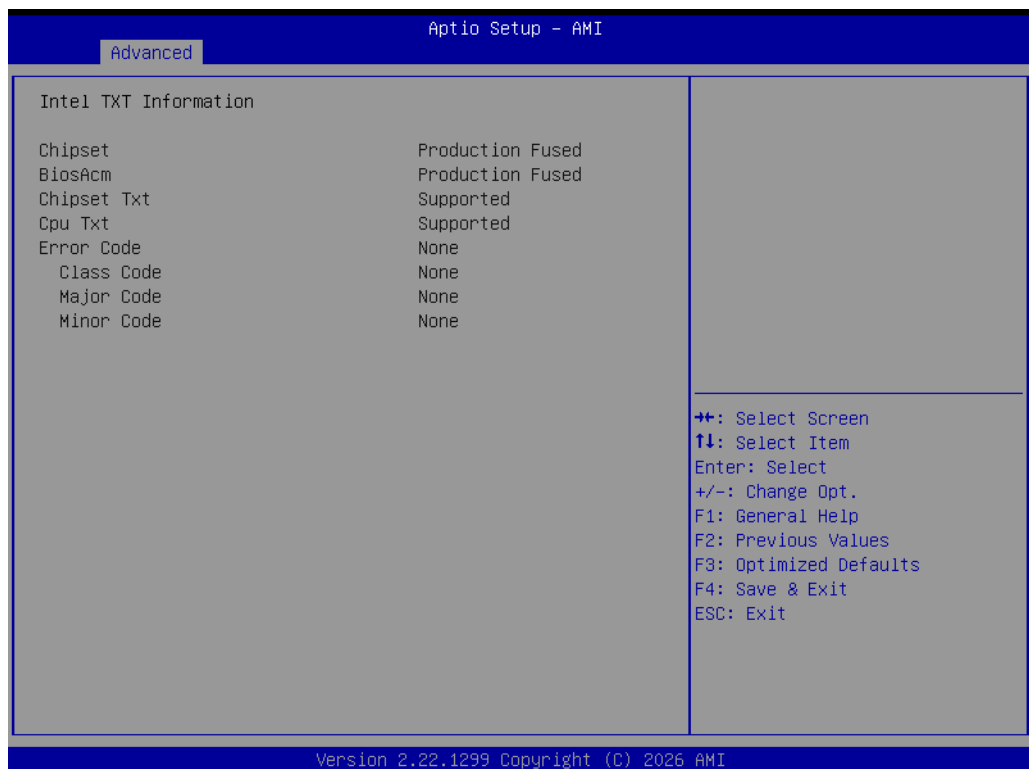
3.2.2.14 Serial Port Console Redirection

Advanced → Serial Port Console Redirection



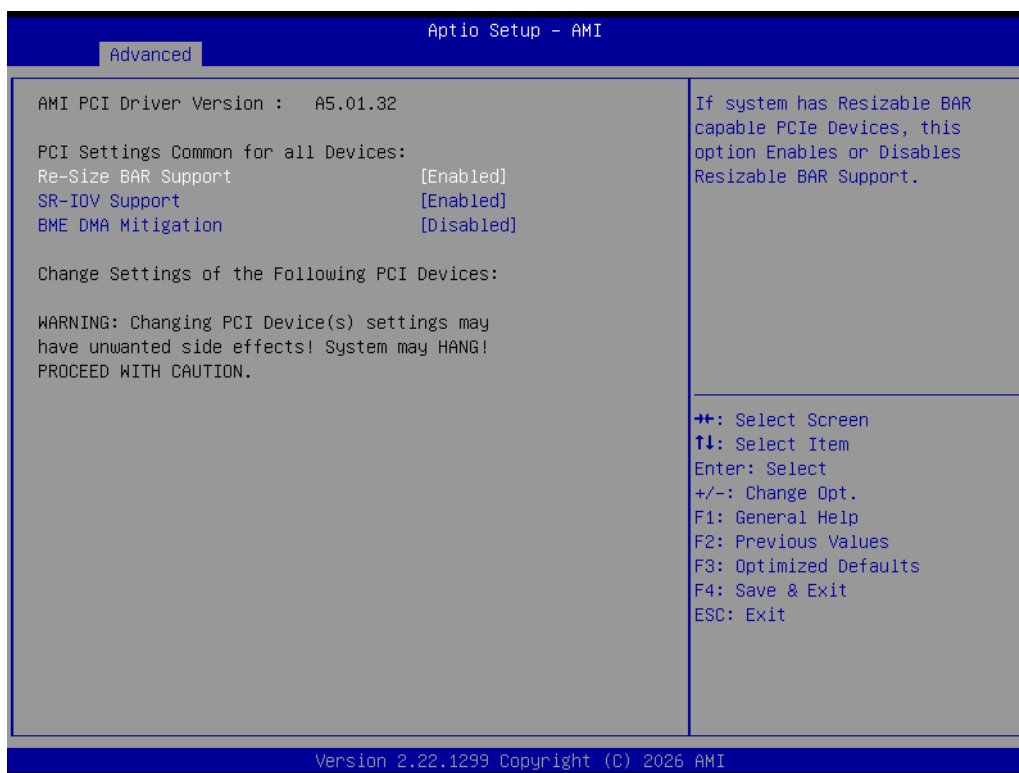
3.2.2.15 Intel TXT Information

Advanced → Intel TXT Information



3.2.2.16 PCI Subsystem Settings

Advanced → PCI Subsystem settings



3.2.2.17 USB Configuration

Advanced → USB Configuration



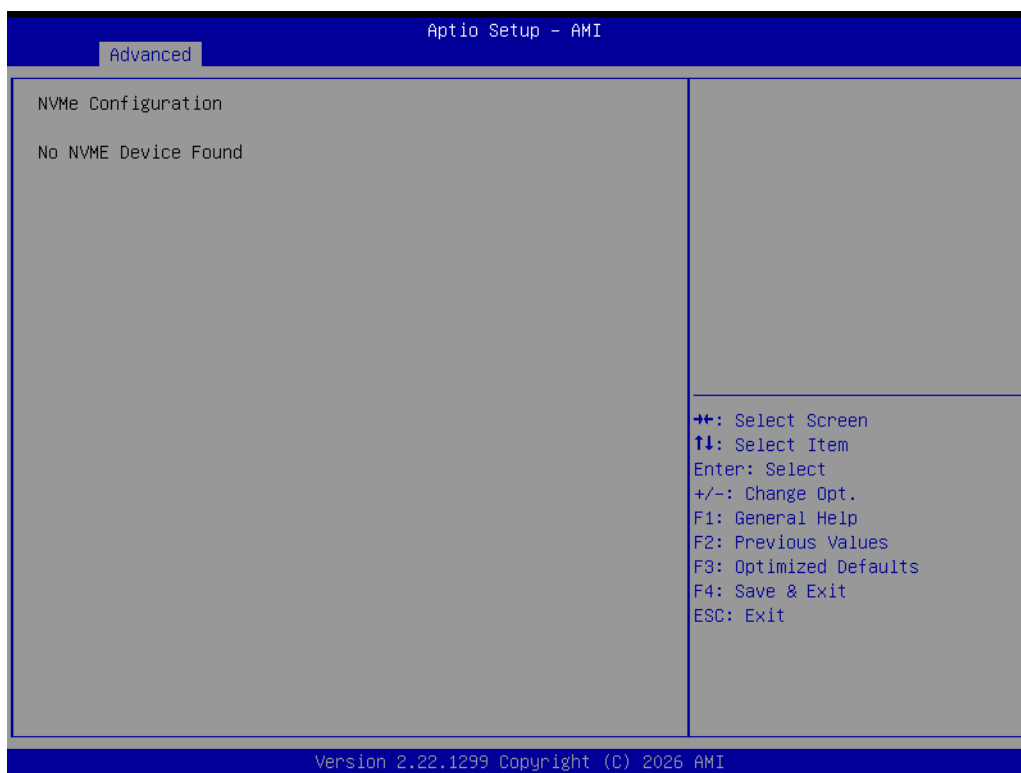
3.2.2.18 Network Stack Configuration

Advanced → Network Stack Configuration



3.2.2.19 NVMe Configuration

Advanced → NVMe Configuration



3.2.3 Security

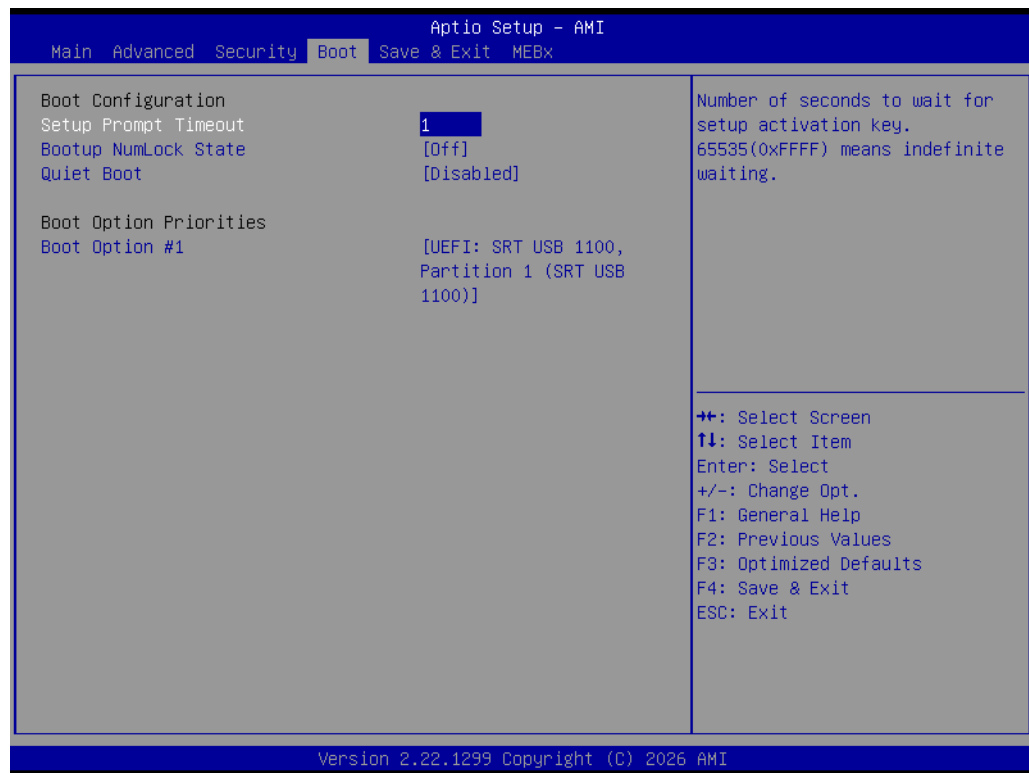


Secure Boot

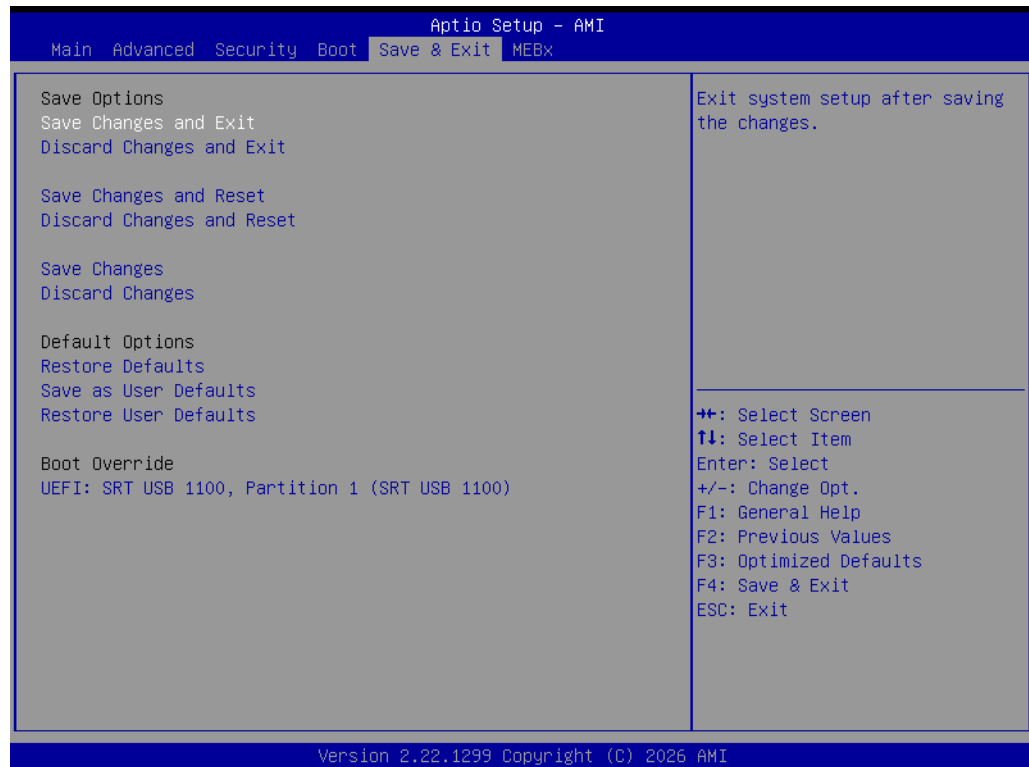
Security → Secure Boot



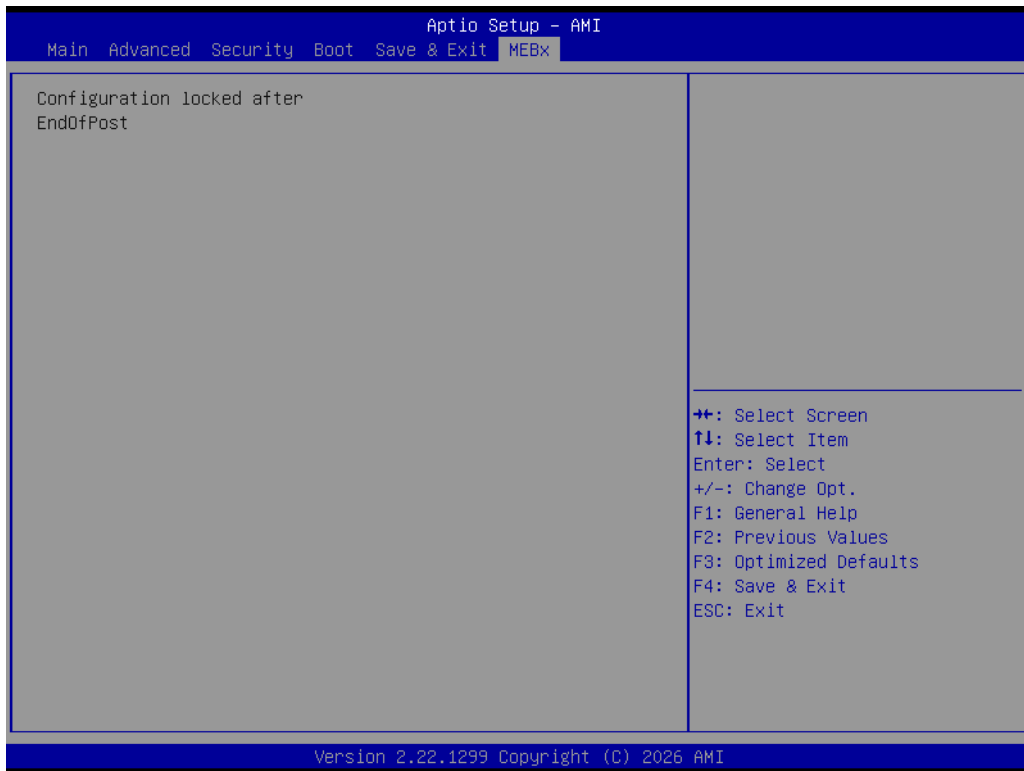
3.2.4 Boot Settings



3.2.5 Save & Exit Configuration



3.2.6 MEBx



Chapter 4

Software Introduction
& Service

4.1 Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft® Windows® embedded technology." We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (hardware suppliers, system integrators, embedded OS distributors) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.2.1 Software API

4.2.1.1 Control

GP I/O



General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provide Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

SMBus



SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

4.2.1.2 Display

Brightness Control



The Brightness Control API allows a developer to access embedded devices and easily control brightness.

Backlight



The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

4.2.1.3 Monitor

Watchdog



A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

Hardware Monitor



The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature and voltage.

4.2.1.4 Power Saving

CPU Speed



Makes use of Intel SpeedStep BIOS technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

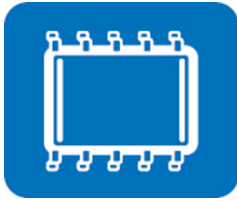
System Throttling



Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

4.2.2 Software Utility

BIOS Flash



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up current BIOS by copying it from the flash chip to a file on customers' disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

Embedded Security ID



The embedded application is the most important property of a system integrator. It contains valuable intellectual property, design knowledge and innovation, but this makes it vulnerable! Embedded Security ID utility provides reliable security functions for customers to secure their application data within the embedded BIOS.

Monitoring



The Monitoring is a utility for customer to monitor the system health, like voltage, CPU and system temperature and fan speed. These items are important to a device, if critical errors occur and are not solved immediately, permanent damage may be caused.

Chapter 5

Chipset Software
Installation Utility

5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for the AIMB-589 are located on the Advantech support website: <http://support.advantech.com/Support/>. The drivers on the support website will guide and link you to the utilities and drivers under a Windows system. Updates are provided via Service Packs from Microsoft*.

Note! *The driver files on the website are compressed. Do not attempt to install the drivers by copying the files manually. You must download the files and decompress them first. Also, please use the supplied SETUP program to install the drivers.*



Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software's user manual before performing the installation.

5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- **Core PCI PnP services**
- **Serial ATA interface support**
- **USB support**
- **Identification of Intel® chipset components in the Device Manager**

Note! *This utility is used for the following versions of Windows, and it has to be installed before installing all the other drivers:*



- **Windows 11 (64-bit)**

Chapter 6

LAN Configuration

6.1 Introduction

The AIMB-589 system features four Gigabit Ethernet LANs via dedicated PCI Express x1 lanes (Lan1: Intel I226-LM V-PRO 2.5 GbE , LAN2: Intel I226-V 2.5 GbE, LAN3/LAN4: Intel I210-AT GbE) that offer a bandwidth of up to 500 MB/sec, eliminating bottlenecks in the flow of network data by incorporating Gigabit Ethernet at 1000 Mbps.

6.2 Features

- Integrated 10/100/1000/2500 Mbps transceiver
- 10/100/1000/2500 Mbps triple-speed MAC
- High-speed RISC core with 24-KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express X1 host interface

6.3 Installation

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*



The Intel I226-LM V-PRO (LAN1), Intel I226-V (LAN2) and Intel I210-AT (LAN3/4) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies between systems. Please follow the driver setup procedure instructions specific to the operating system installed.

6.4 Windows® 11 Driver Setup

Download the driver from support website on your computer and decompressed the file. Select the “Autorun” then navigate to the directory for your OS.

Note! *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*



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